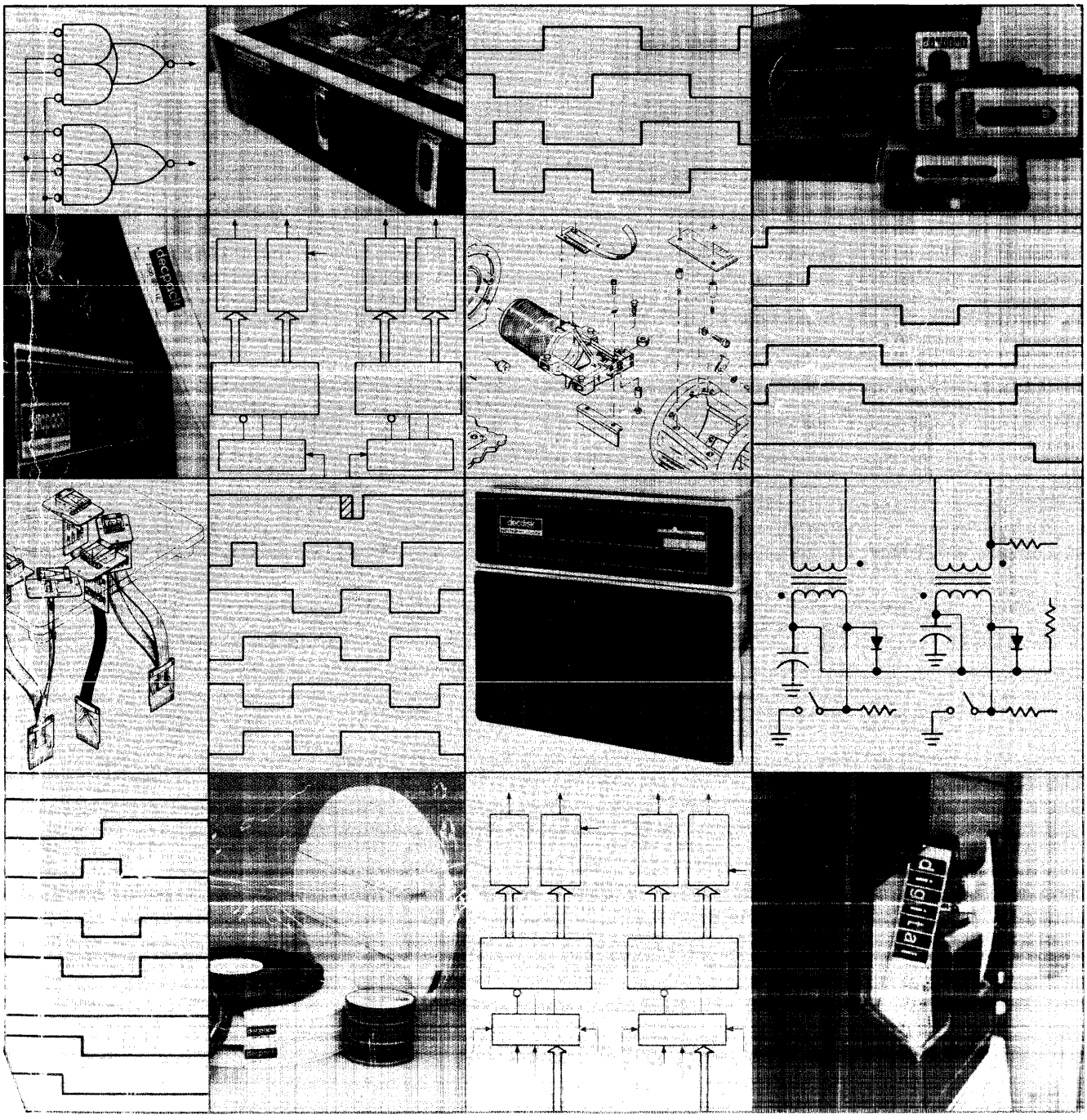
digital

RK6/7 FTB
operating and service manual



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operating and service manual

EK-RK67F-OP-001

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PREFACE

This manual describes the RK6/7 Field Test Box (FTB). The FTB is designed to test, exercise, and perform off-line head alignments. Also included is information detailing operator controls and indicators, head alignment, and troubleshooting techniques for testing and isolating disk drive malfunctions.

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The RK6/7 FTB is a self-contained, portable suitcase tester designed to test and exercise an RK06 or RK07 disk drive off-line directly through the drive's interface hardware. The FTB also provides the user with a method of testing and aligning an RK06 or an RK07 disk drive with or without a processor. When used in conjunction with the system head alignment diagnostic, it provides the user with a method of performing on-line alignment verifications.

CAUTION

If a formatted disk pack is used in conjunction with the FTB for testing puposes, the disk format will be destroyed (written over) and the pack will have to be reformatted before it can be used for on-line data usage.

All write/read data transmissions, disk drive commands, and status messages are connected from the FTB to the drive via a standard interface cable. A separate cable, adapter, and preamplifier assembly connect the FTB directly to the drive's write/read module for head alignment.

The FTB is configured so that the head alignment logic is functionally independent from the tester's interface logic. This feature allows on-line head alignment (without disconnecting the controller/drive interface cable) using the head alignment diagnostic to run the drive and the FTB to monitor the readings using the head alignment meter.

NOTE

In order to realize the full potential of the FTB, the user should have a thorough understanding of the controller/drive interface logic of both the RK06 and the RK07 drive. Refer to the RK06/RK07 Disk Drive Technical Description Manual (EK-RK067-TD-001).

1.2 CAPABILITIES OVERVIEW

The FTB is designed around a repetitive loop concept (basic loop) that can be modified through front panel controls by the operator. The basic loop is designed to put the disk drive through complex write/read exercises that test both electrical and mechanical operations of the drive. The basic loop causes the write/read heads to be positioned on all cylinders, to write data on and read data from all tracks and sectors of the disk pack (simulates system operation), and to check for errors.

The versatility of the FTB is a direct result of the flexibility by which the basic loop can be modified by the operator. The options that can be selected via the front panel controls are:

- Halt on errors/ignore errors
- Address a specific cylinder
- Address a specific head
- Positioning only
- Read only
- Write only
- Status reporting
- Continuous/single cycle operation
- Sync on FTB clock (INT) or drive clock (WRCLK)
- Address all sectors or sector 0 only
- Run interface FAST (normal mode) or SLOW (for scoping ease).

In addition to these features, the FTB contains design features that allow the user to diagnose problems in the drive's logic that are very difficult for the system's diagnostics to test. These special features are as follows.

- Generates A and B parity errors independently
- Generates a multiple drive select (MDS) condition
- Generates a controller power-off condition
- Provides a synthetic clock (INT) for test use in case the drive's WRCLK is not working correctly or is inoperative
- Provides two speeds for interface operation for scoping ease

1.3 REFERENCE DOCUMENTS

It is recommended that the following documents be reviewed prior to using the FTB under actual test conditions.

EK-RK067-UG-001	RK06/RK07 Disk Drive User's Manual
EK-RK067-TD-001	RK06/RK07 Disk Drive Technical Description Manual
EK-RK067-SV-001	RK06/RK07 Disk Subsystem Service Manual
EK-RK06-IP-001	RK06 IPB Manual
EK-RK07-IP-001	RK07 IPB Manual

CHAPTER 2
UNPACKING AND ACCEPTANCE TESTS

2.1 SCOPE

The following paragraphs include unpacking and basic acceptance test procedures.

2.2 UNPACKING PROCEDURE

1. Remove the suitcase (carrying case) from the shipping carton and perform a visual inspection for any signs of damage. Damage claims should be forwarded to the responsible shipper.

2. Release and open the carrying case cover. Perform a visual inspection to ensure no physical damage is evident and that there are no broken controls or indicators.

3. Release and open the tester's control panel so that internal components can be inspected (Figure 2-1). Check for loose or broken wires and ensure that the printed circuit boards are seated properly and are installed in the proper location.

4. Check the equipment tag on the lower right corner to ensure that the unit lists the proper line voltage and correct model number (as ordered).

NOTE

Model RK6/7-TA is 115 V, 50/60 Hz; Model RK6/7-TB is 230 V, 50/60 Hz.

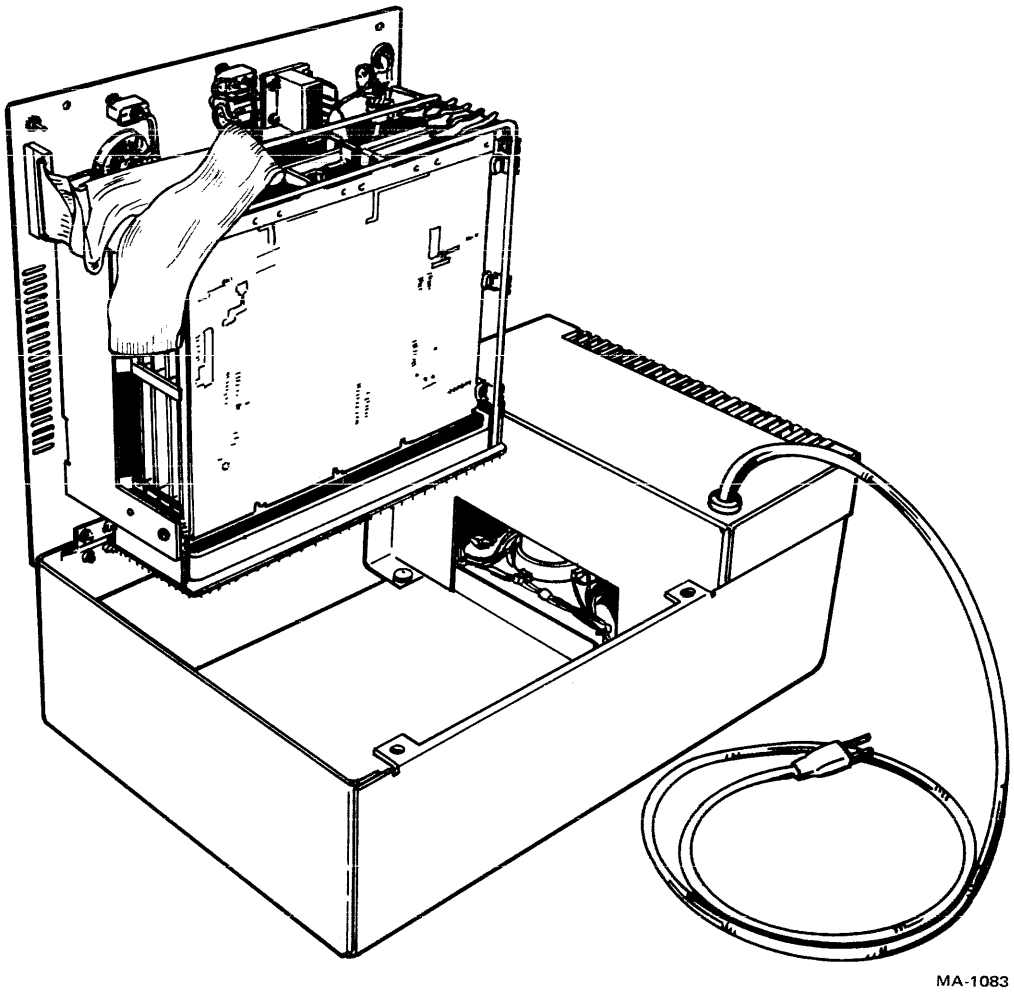


Figure 2-1 Field Test Box (Internal View)

2.3 ACCEPTANCE TESTS

The RK6/7 Field Test Box is thoroughly tested and certified at the factory before it is shipped. Therefore, the following acceptance tests are designed to reaffirm that there was no damage to the tester's electronics during shipping and handling.

NOTE

If any faults are detected in the following procedures, refer to Chapter 5 and correct the fault before proceeding to the next step.

1. Remove the printed circuit boards from the tester.

2. Connect the tester's line cord to a convenient wall receptacle and turn the tester's ON/OFF switch to the ON position.

3. Check the following pins on the wired backplane (Figure 2-2) for the correct voltage levels.

Pin	Voltage Level	Pin	Voltage Level
A1A2	+5 V	D1B2	-15 V
A2A2	+5 V	C4B2	-15 V
A3A2	+5 V	D1R2	-5 V
A4A2	+5 V	B3F2	-5 V
D1D2	+15 V	D3F2	-5 V
D3D2	+15 V	A4R2	-5 V
A4D2	+15 V		
C4D2	+15 V		

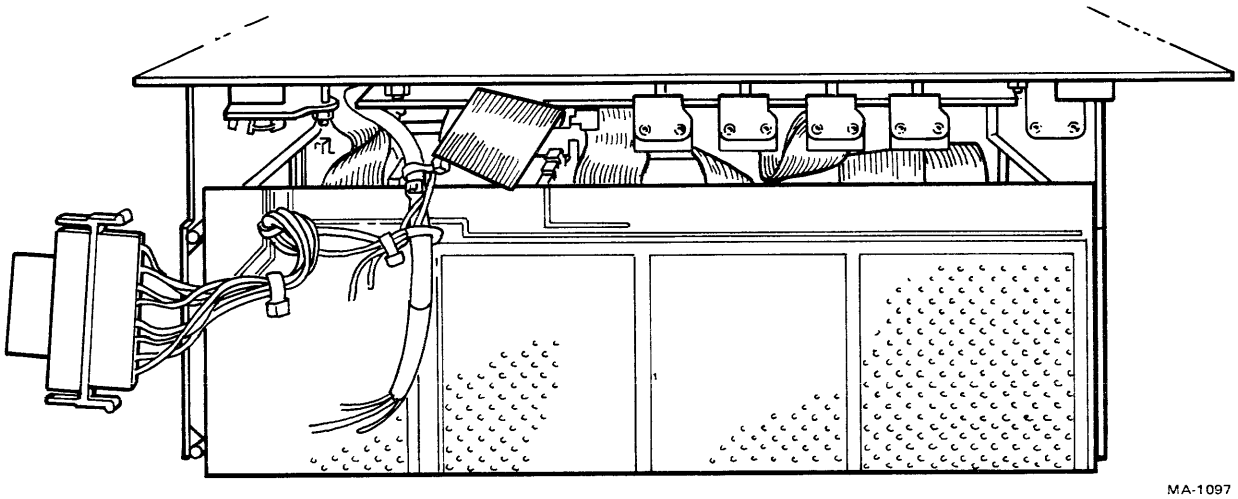


Figure 2-2 Field Test Box Backplane

4. Turn tester off and disconnect line cord.

5. Disconnect the dc power cable between the backplane and the power supply.

6. Install printed circuit boards into tester and check resistance from voltage pins to ground. A list of the approximate resistance levels that can be expected when measuring from voltage pins to ground is as follows.

Voltage Pin	Resistance Level
+5 V +15 V -15 V -5 V	Between 0Ω and 10 KΩ

7. Reconnect the dc power cable between the backplane and the power supply.

8. Install printed circuit boards (Figure 2-1).

9. Refer to Chapter 5 and perform the off-line checkout procedures outlined in that chapter.

CHAPTER 3
CONTROLS AND INDICATORS

3.1 SCOPE

This chapter describes the function of each front panel control and places special emphasis on how the user can vary the basic loop function. Where applicable, potential uses for deviating from the basic loop function will be described.

3.2 OPERATOR CONTROLS

Figure 3-1 and Table 3-1 illustrate and define the RK6/7 FTB controls and indicators. It should be noted that the basic loop configuration (except for cylinder switch register switches 2^0–2^9) consists of putting all applicable switches in the underlined positions as indicated on the control panel. The cylinder switch registers (SWR) that are underlined denote cylinder address 245. This defines the cylinder address which is used during head alignment on an RK06 drive, when an RK06K-AC alignment pack is installed in the drive. The cylinder switch registers that have dots underneath them denote a cylinder address of 496. This defines the cylinder address that is used during head alignment on an RK07 drive, when an RK07K-AC alignment pack is installed in the drive.

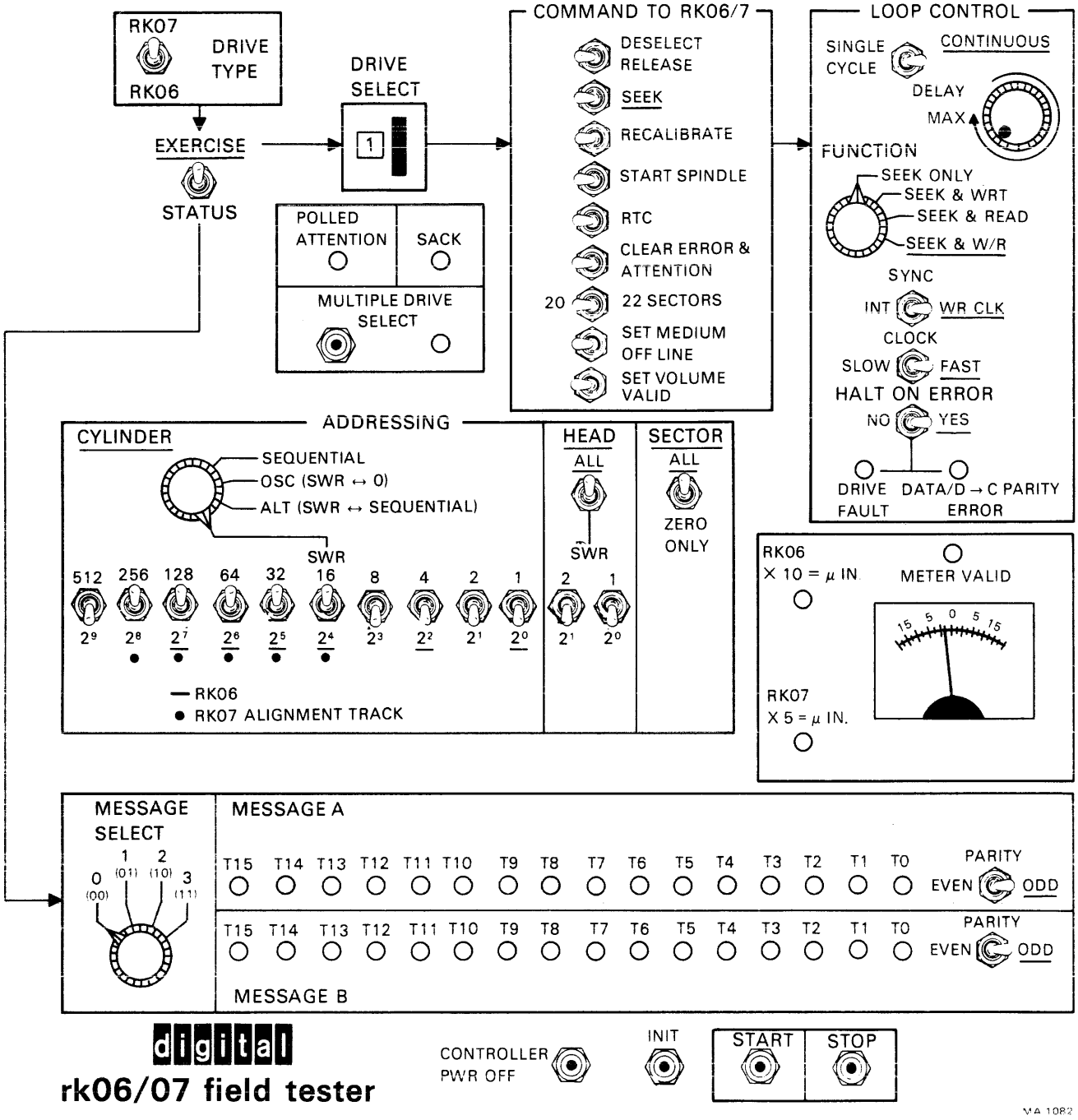


Figure 3-1 Field Test Box Controls and Indicators

Table 3-1 Controls and Indicators

Switch Indicator	Function
DRIVE TYPE RK06	Puts FTB in mode for testing RK06 disk drive
RK07	Puts FTB in mode for testing RK07 disk drive
EXERCISE/STATUS	In the exercise mode, the tester sends the drive a message, receives MESSAGES A and B (T0–T15) from the drive, checks for a drive-to-tester Parity Error or a Drive Fault and then a Drive Ready. This is done repetitively until a Drive Ready is generated by the drive and sent to the FTB. When Drive Ready is received, the write process starts followed by a read. If any data errors are found during a read operation, the error is stored and the cycle continues until the revolution is completed; then it halts operation. In status mode, the tester formulates a drive message which requests a return of the message to the FTB as set in the MESSAGE SELECT switch, transmits the message once, receives back the requested message, and displays it in the MESSAGE A and MESSAGE B LEDs and halts. **Potential Uses:** If the tester halts on a Drive Fault error in the exercise mode, status mode may be selected, and START pushed to display any of the eight message lines (as determined by the SELECT switch positions). The MESSAGES A and B LEDs can be consulted to determine the specific error generating the DRIVE FAULT condition.
DRIVE SELECT	The DRIVE SELECT switch is used to select the drive number (under test) to which messages will be transmitted. The DRIVE SELECT switch also determines which drive number will be transmitted on the polled address interface lines (i.e., 2^0, 2^1, and 2^2).
POLLED ATTENTION	The POLLED ATTENTION LED indicates the condition of the POLLED ATTENTION interface line. If the drive, whose address is in the DRIVE SELECT switch, has attention set, the LED will light. **NOTE** **The LED will appear to be lit all of the time. However, the 2^0 POLLED ADDRESS line sent to the selected drive is inverted for a very short time in order to toggle the drive logic and to facilitate scoping for troubleshooting purposes.**

Table 3-1 Controls and Indicators (Cont)

Switch/Indicator	Function
SACK	The SACK LED displays the condition of the SELECT ACKNOWLEDGE line transmitted by the drive. It will light after the drive number (set in the DRIVE SELECT switch) is transmitted to the drive. The SACK LED will only light if the DRIVE SELECT switch matches the number in the FTB DRIVE SELECT switch and if the deselect/release bit is negated.
MULTIPLE DRIVE SELECT	The MULTIPLE DRIVE SELECT LED displays the state of the MULTIPLE DRIVE SELECT line, transmitted by the drive. The LED will light when the MULTIPLE DRIVE SELECT button is pushed. Pushing the button causes the tester to assert the INDEX-SECTOR line. When sensing INDEX and SECTOR assertions other than its own, the drive under test will detect a MULTIPLE DRIVE SELECT message, assert the MULTIPLE DRIVE SELECT line, and light the LED.
COMMAND TO RK06/7 **NOTE** **The next nine switches in the COMMAND TO RK06/7 block set message bits which the tester sends to the drive in message A, bits T3 through T11.**	
DESELECT/RELEASE	The DESELECT/RELEASE command sets the drive available status bit to the other controller in dual-access system configuration. The drive is deselected when this bit is asserted. A request may be cancelled via a message containing a DESELECT/RELEASE command. Note that no message line status information is received when such a command is issued.
SEEK	This command directs the drive to seek to the cylinder address transmitted on MESSAGE LINE B. The selected binary-encoded address is transmitted to the drive with the least significant bit first.
RECALIBRATE	This command directs the drive to seek to cylinder number 0 and to reset the cylinder address register. This command is used to resynchronize the drive position with its electronics if for any reason it gets out of step.

Table 3-1 Controls and Indicators (Cont)

Switch/Indicator	Function
START SPINDLE	This command directs the drive to start its spindle and subsequently to perform a brush cycle and load heads if and only if the RUN/STOP switch on the front panel is depressed (RUN). The START SPINDLE command can be used to restart a drive in the event that a SET MEDIUM OFF LINE command has caused the heads to unload or any of the error conditions that unload heads has occurred. Under such conditions, the error must be cleared before this command will allow the heads to reload.
RTC	The return-to-centerline (RTC) command is used to reset head offsets when a write operation is to take place. The clearing of the offset mode requires 3 ms to complete at which time a DRIVE ATTENTION is transmitted to the FTB. An RTC command is implied by any non-zero cylinder seek or upon detection of a write gate in the event that an RTC command is not detected.
CLEAR ERROR & ATTENTION	When the CLEAR ERROR & ATTENTION command is asserted, it clears the drive status change flip-flop (DRIVE CLEAR) as well as clearing all error flags in the selected drive provided that the errors no longer exist.
20/22 SECTORS	This bit, when asserted, commands 20 sector pulses per disk rotation; when not asserted, 22 sector pulses are commanded. Twenty sectors correspond to 18-bit data words; 22 sectors correspond to 16-bit data words. Whenever a change in the format is made with this select bit, sector pulses cease, until the next sector 0 at which time the drive is synchronized to the new format.
SET MEDIUM OFF-LINE	This bit, when asserted, unloads the drive heads and stops the spindle.
SET VOLUME VALID	This bit, when asserted, sets the volume valid flip-flop, thereby acknowledging a power turn-on, change of cartridge, or the removal of the unit select plug.
LOOP CONTROL NOTE **All switches in the LOOP CONTROL block (upper right of panel) allow modification of the basic loop mode of system operation.**	

Table 3-1 Controls and Indicators (Cont)

Switch/Indicator	Function
SINGLE CYCLE/ CONTINUOUS	If this switch is moved from the continuous mode to the single cycle mode, a command is formulated and messages are continuously transmitted and received until DRIVE READY is asserted. Writing and reading are done, errors are checked, and a new command is formulated in the tester but is not transmitted. In the single cycle mode, the new message is sent only when the START pushbutton is pressed, (i.e., repetitive operations in the single cycle mode must be manually initiated by repetitive activation of the START switch.) **Potential Uses:** 1. To write on only one track of the disk and have the writing stop at a track boundary. **CAUTION** **Pushing the STOP pushbutton would stop operations instantly and thus could cause an error in the current sector because writing could cease in the middle of a sector.** 2. If positioning problems are encountered which cause the drive to shut itself down, the single cycle feature provides a method to manually initiate seeks at a very low rate while scoping the logic.
DELAY	The DELAY knob is an adjustable time delay control that delays tester recognition of DRIVE READY from approximately 220 μs to approximately 700 ms. Thus, it offers a method of adjusting the time between completion of a SEEK and the initiation of a WRITE/READ. **Potential Uses:** 1. If the settling time of the servo is taking longer than recommended, increasing the delay before writing could eliminate the data errors and thereby indicate a possible clue to the problem source. 2. If a problem exists that causes the drive to cease operation, a long delay between SEEKS will provide additional time for scoping before the drive stops. 3. Any unwanted resonances could be isolated by varying (tuning) the time delay between seeks.

Table 3-1 Controls and Indicators (Cont)

Switch/Indicator	Function
FUNCTION	The FUNCTION switch is used to modify basic loop operations involving positioning, writing, and reading. The modifications (to the basic loop) offered by this switch involve SEEK ONLY, SEEK & WRT, SEEK & READ, and SEEK & W/R. **Potential Uses:** The positions are useful when working on positioning problems not involving reading or writing, or when working on data problems to separate write problems from read problems.
SYNC INT/WR CLK	In the basic loop mode, the clock source is the interface write clock which is generated by the drive disk pack. Because difficult-to-detect problems with write clock can cause random data errors, write clock accuracy is critical and imperative to proper read/write operation of a drive. **Potential Uses:** To help isolate random data errors, the SYNC switch can be put in its INT position. This causes the tester to use an internal oscillator as a system clock and to ignore the interface write clock. In summary, if random data errors are occurring, and switching to SYNC/INTernal stops the errors, write clock problems should be suspected.
CLOCK SLOW/FAST	The main clock on the interface clocks status and command information between the FTB and the drive. In the fast mode, the control clock repetition rate is at standard system speed (465 ns/cycle) and in the slow mode, control clock rate is 29.8 μs/cycle. Slow speed enhances scoping and is also useful in detecting speed problems.
HALT ON ERROR NO/YES	The HALT ON ERROR switch is self-explanatory. The DRIVE FAULT LED is lit (in exercise mode only) whenever the interface drive fault bit is asserted by the drive. Simply, this LED indicates an error detected by the drive. The DATA/D→C PARITY ERROR LED indicates any error detected by the tester. These may be of two types. 1. Data error (if FUNCTION includes a read) 2. Drive-to-tester parity error. **NOTE** **To aid in debugging intermittent problems, the LEDs will light when errors exist independent of the setting of the HALT ON ERROR switch.**

Table 3-1 Controls and Indicators (Cont)

Switch/Indicator	Function
ADDRESSING **NOTE** **The ADDRESSING block provides many addressing variations from the basic loop operation addressing scheme previously described.**	
SEQUENTIAL	Successive cylinder addresses may be SEQUENTIAL cylinder addressing, which positions the drive to the address in a register that is incremented by 1 every cycle (one complete basic loop cycle). Example: (RK06) 0, 1, 2, 3 . . . 410, 0, 1, 2. . . Example: (RK07) 0, 1, 2, 3 . . . 814, 0, 1, 2 . . .
OSC (SWR ↔ 0)	Oscillate cylinder addressing positions the drive between cylinder 0 and a cylinder number set in the switch register. Example: 0, (SWR), 0, (SWR), 0, (SWR), 0, (SWR) . . .
ALT (SWR ↔ SEQUENTIAL)	ALT (SWR ↔ SEQUENTIAL) cylinder addressing positions the drive between the switch register address and an address in a register that is incrementing by one every other basic loop cycle. Example: 0, (SWR), 1, (SWR), 2, (SWR), 3, (SWR) . . .
SWR	SWR cylinder addressing positions the drive to the address in the switch register (and does not change the cylinder address on sequential loop cycles). **NOTE** **In the SWR mode, successive messages call for the same cylinder (contained in the switch register) and allow repetitive writing and reading without performing any SEEKS.**

Table 3-1 Controls and Indicators (Cont)

Switch/Indicator	Function
HEAD ALL/SWR	When the HEAD switch is placed in the ALL position, it causes all the heads (0, 1, and 2) to write and read on the selected cylinder in the following sequence after the seek is complete: Write head 0, read head 0 Write head 1, read head 1 Write head 2, read head 2 Seek to new cylinder address Write head 0, read head 0, etc. When the HEAD switch is placed in the SWR position, it causes only the head selected by switches 2^0 and 2^1 to be used for write and/or reading. **NOTE** **Any head (0, 1, or 2) can be selected using the HEAD SWR switches. The function performed depends on the FUNCTION switch position.** **NOTE** **The LEDs under the cylinder and head switch registers always display the last cylinder and head addresses sent to the drive.**
SECTOR ALL/ZERO ONLY	Sectors that are to be written and read may be ALL sectors (20 in 20-sector mode or 22 in 22-sector mode) or sector ZERO ONLY.
MESSAGE SELECT	When the tester is in the exercise mode, the FTB requests and receives messages A0 and B0 only from the drive. This allows the tester to monitor Drive Ready and Drive Fault for errors. If an error message is detected and/or the user wants to view the contents of the other message lines (1, 2, or 3), the status mode can be selected. Upon actuation of the START button, the FTB requests and receives the message line selected by the MESSAGE SELECT switch. The selected message line status/error bits are then displayed in the MESSAGE A and MESSAGE B LEDs. The message lines A1–A3 and B1–B3 will provide more specific status/error information concerning the composite error/status that was indicated in the exercise mode in messages A0 and B0.

Table 3-1 Controls and Indicators (Cont)

Switch/Indicator	Function
PARITY ODD/EVEN	The MESSAGE A and MESSAGE B PARITY switches cause the tester to transmit wrong (EVEN) parity to the drive independently on MESSAGE A and B lines to ensure that the drive can detect these errors.
CONTROLLER PWR OFF	The CONTROLLER PWR OFF button is used to verify that the drive is capable of sensing this line in case a real power loss occurs at the controller. This interface line is also connected to the +5 V in the FTB to disable the interface in case tester power is lost.
INIT	The INIT button generates an assertion on the initialize interface line. It performs the same function as the controller initialize command.
START/STOP	The START and STOP switches start and stop commands and data from the tester. Operation is not guaranteed if switches are changed without stopping the tester first. STOP clears the tester, and all addressing, etc., and will start at an initialized state when START is pressed and released. If the tester halts on an error, status may be checked by selecting STATUS and repeatedly pushing START without pushing STOP. In this case, the tester-formulated message will not change. In the single cycle mode, repetitive STARTs will increment the tester whereas a STOP will initialize the tester.

CHAPTER 4
UTILIZATION

4.1 SCOPE

This chapter stresses general and special operating procedures and describes both the basic loop and interface principles that are incorporated into the RK06/7 FTB. Also included in this chapter are basic setup (cabling and connections) and head alignment procedures.

4.2 BASIC LOOP DESCRIPTION

The basic loop setup is the most complicated and thorough test that can be used to exercise and test a good device drive.

In this mode, the tester sends the drive a message as defined by COMMAND TO RK06/7 and LOOP CONTROL switch selections and receive status messages in MESSAGE A and MESSAGE B LEDs (lines A0 and B0) from the drive. The tester checks for a drive-to-tester Parity Error, a Drive Fault, and then a Drive Ready. These steps occur repetitively until a Drive Ready flag is asserted at which time the selected track is written and read and checked for errors. If no errors are present, the tester generates the next command. Repetitions of this cycle provide a method of sequencing through all sectors of all tracks of all cylinders and in that order.

Each cycle monitors and indicates any Drive Fault errors (line B0, bit T7) and any tester-detected errors (DATA/D→C PARITY ERROR). The operator can choose to HALT ON ERROR (YES) or to ignore an error HALT ON ERROR (NO) and continue the repetitive loop cycle.

High and low frequency patterns (only) will be alternately written in odd and even sectors. These frequency patterns provide a method of checking the recovery system within its specified frequency range and to qualify write/read system performance by scoping the ratio between the high and low frequency amplitudes.

4.2.1 Status Reporting

The FTB can be switched into the status mode at any time (after pushing STOP) for the purpose of examining the status/error bits in the MESSAGE A and B LEDs (words 00, 01, 10, and 11).

NOTE

In the exercise mode, message words A0 and B0 are always monitored because they contain the composite Drive Ready and Drive Fault bits which are necessary for basic loop operation.

In the basic loop mode of operation, if a composite error bit is received, the FTB halts on the error and displays the bit in the MESSAGE A0 or B0 LEDs. The operator then switches the FTB into the status mode and views the words received from the drive to determine what error bit(s) caused the composite error. Figure 4-1 illustrates the 8-word status messages. A more detailed description of these messages is given in Appendix A.

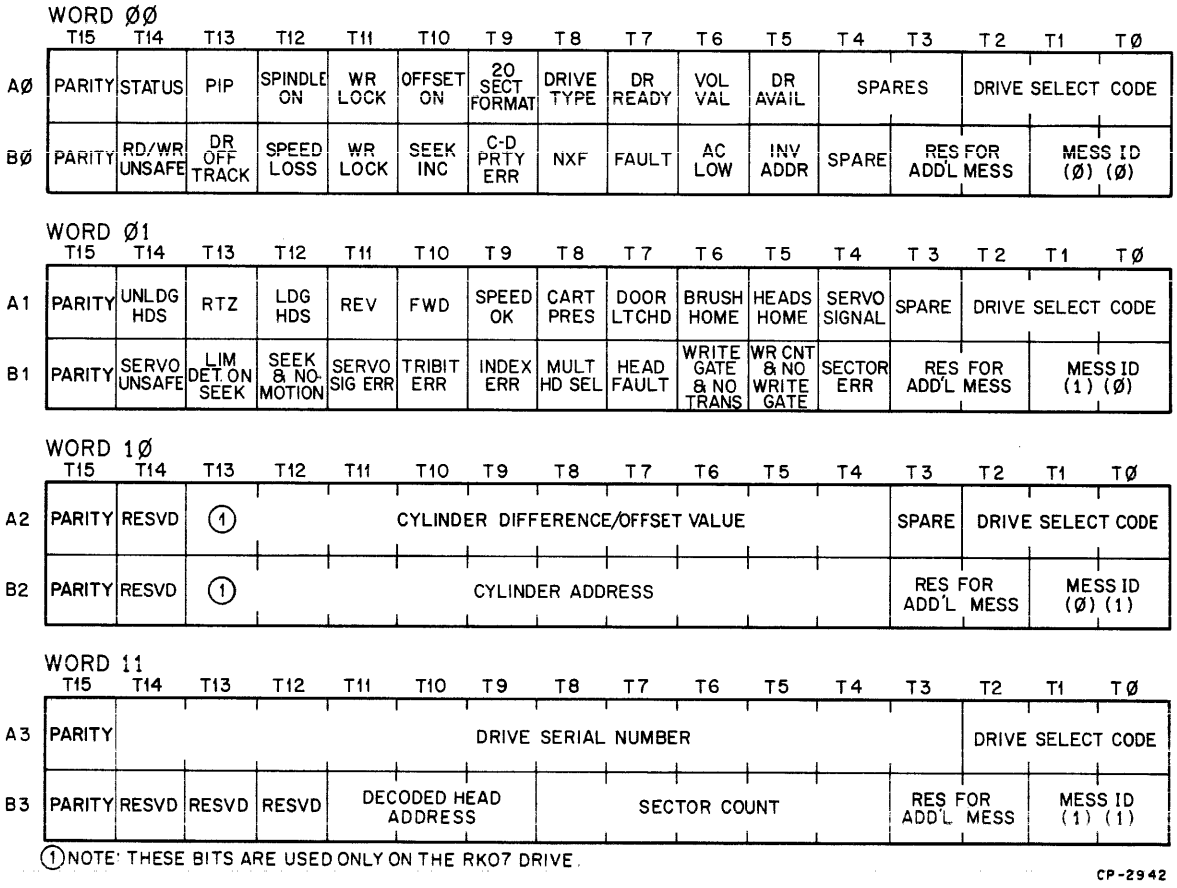


Figure 4-1 MESSAGES A and B Status Indicators

4.2.2 Interface Description

Communication between the FTB and the drive under test is accomplished via a 17-signal serial data and control signal interface cable. Signals for drive selection, commands, addressing, and status reporting are handled serially on two signal pairs, message lines A and B (Figure 4-2). The remaining lines consist of read/write data, timing and control, and attention flag signals.

4.3 CABLING SETUP PROCEDURES

The FTB is connected to the disk drive via the A or B port bus interface. Thus, when the tester is connected to either interface, the corresponding access switch (A or B) on the drive's front panel must be enabled (pressed in) and the other switch must be disabled. Depending on the access port (A or B) being used in the system configuration, an M7706 Interface and Timing logic module will be in slot 2 (B port) or slot 3 (A port). Refer to Figure 4-3.

In the case of a dual access drive system configuration, one of the daisy-chain bus interfaces (A or B) must be temporarily disconnected so that the tester can be connected. In this configuration, one of the controllers and one disk subsystem will be disconnected until the tester box and cabling are removed and the system configuration is returned to normal.

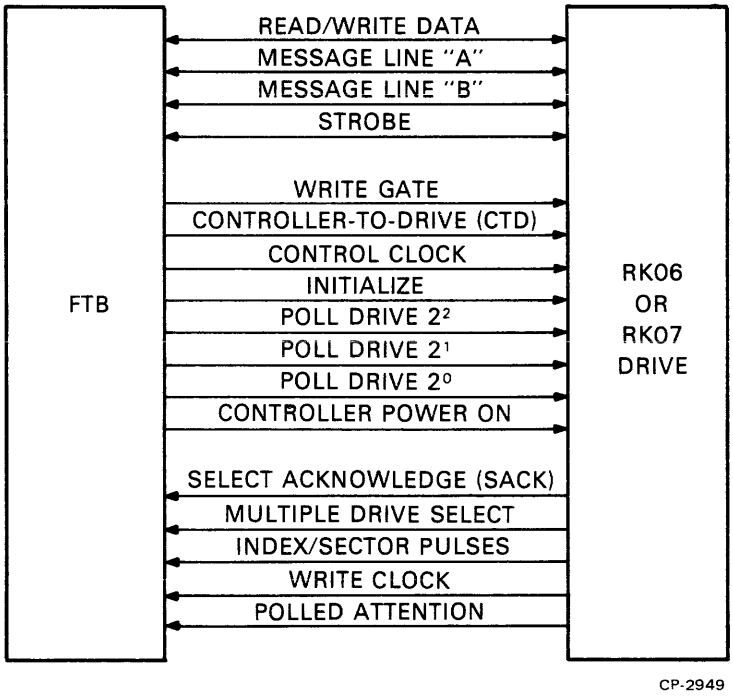


Figure 4-2 FTB/Drive Interface Lines

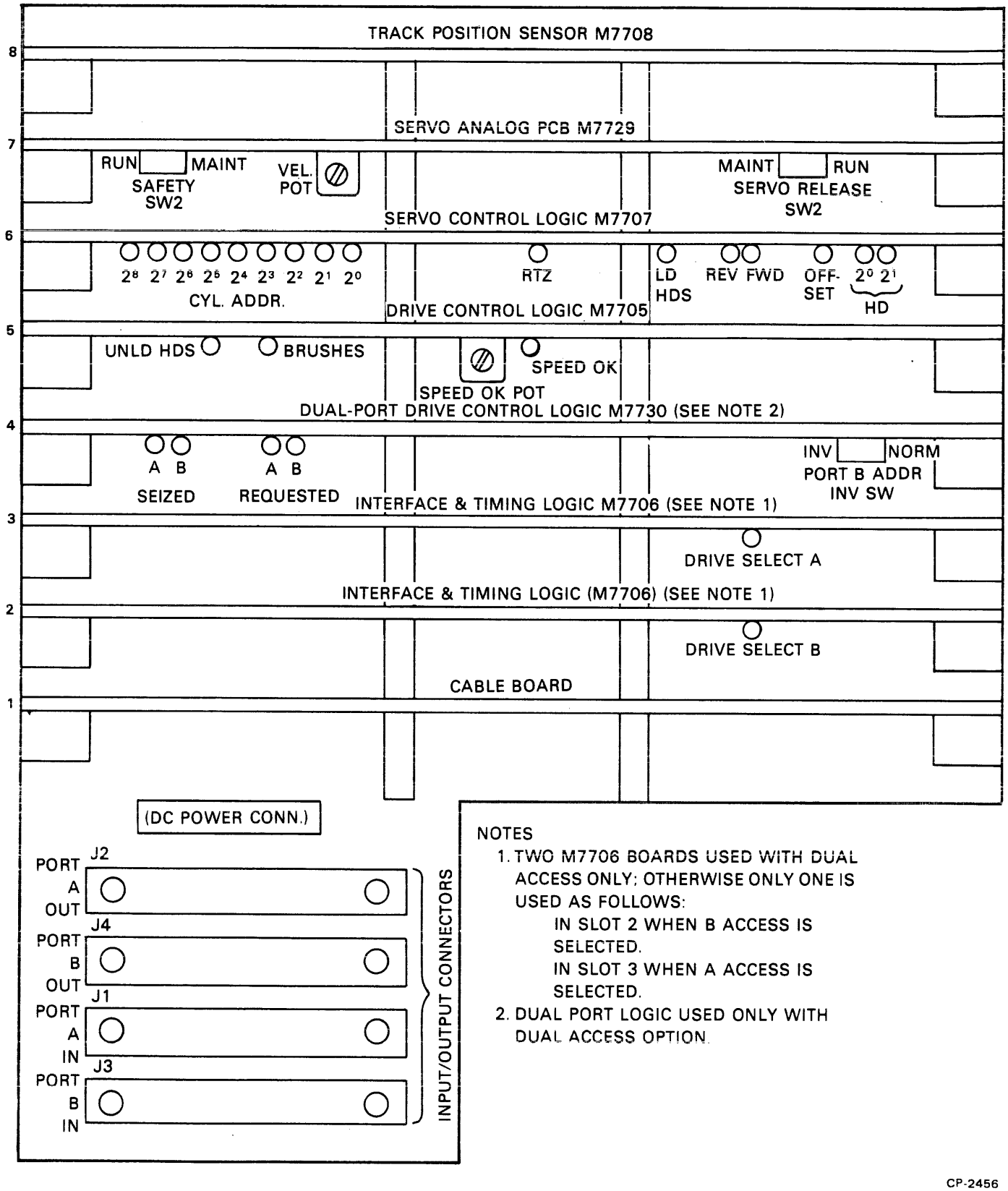


Figure 4-3A Drive Module/Slot Layout (RK06 Drive)

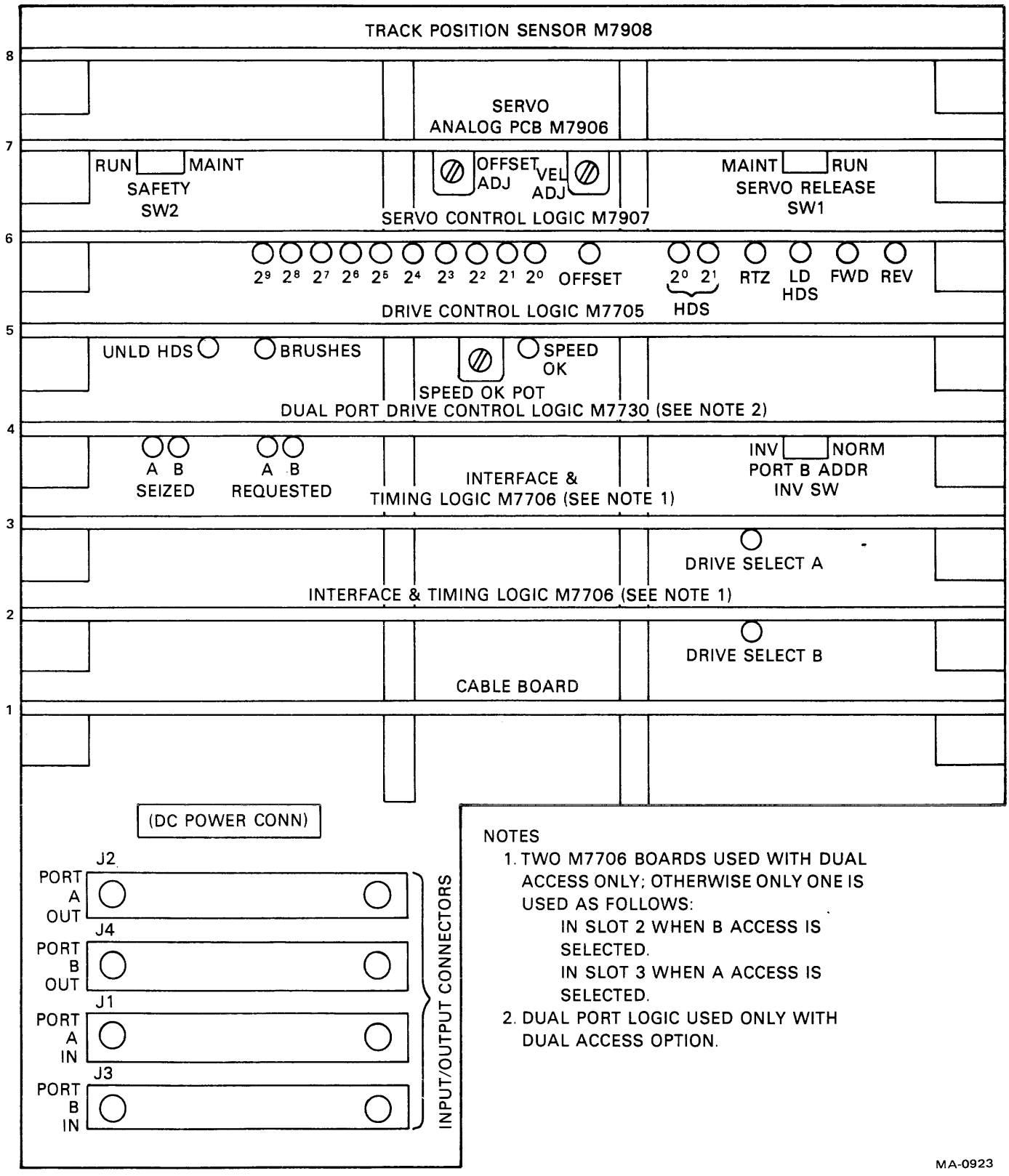


Figure 4-3B Drive Module/Slot Layout (RK07 Drive)

4.3.1 Single Port RK06 or RK07 Setup Procedure (without uncabling system)

1. Disable the port currently in use.
2. Press the RUN/STOP pushbutton on drive to the STOP position.
3. Turn power off to the disk drive.
4. Remove the rear cover from the disk drive unit.
5. Pull the card cage open (out and downward) and inspect logic to determine which port (A or B) is currently being used in the system configuration.
6. Remove the M7706 module and install it in the alternate slot position (i.e., if A port is used, remove M7706 from slot 3 and install in slot 2 for B port.)
7. Connect "spares" interface cable to PORT B IN (J3B) on the INPUT/OUTPUT connectors.
8. Connect "spares" terminator block into PORT B OUT (J4B).
9. Connect the other end of the "spares" interface cable to connector on FTB front panel.
10. Turn on power to the disk drive.
11. Remove system data disk pack from drive.
12. Install a known good scratch pack into drive.
13. Push B port switch in (the new port just cabled up to the FTB).

NOTE
This will be access switch A if PORT A IN is used in steps 4, 5, and 6.

14. Connect the FTB's line cord to the same ac power source as that of the drives.
15. Refer to Paragraph 4.4 for operating instructions.

4.3.2 Dual Port RK06 or RK07 Setup Procedure (without uncabling system)

In the following procedure, it is assumed that this is the initial setup procedure for a dual port system. Therefore, many of the steps outlined in the single port setup procedure (Paragraph 4.3.1) are also listed here for clarity purposes in cabling a dual port system. It should be noted that a dual port system consists of two controllers with up to eight drives on each controller. Thus, one controller and all of its drives will be disconnected to faciliate testing of the drive.

1. Press the RUN/STOP pushbutton on the drive (to be tested) to the STOP position.
2. Turn off power to the disk drive.

3. Remove the rear cover from the disk drive unit.

4. Pull card cage out and downward.

5. Remove daisy-chain cable from PORT A IN (J1A) or from PORT B IN (J3B).

6. Connect "spares" interface cable into the selected port (PORT A IN or PORT B IN).

7. Connect "spares" terminator block into selected port out connector (PORT A OUT OR PORT B OUT).

8. Connect the other end of the "spares" interface cable into the connector on the FTB front panel.

9. Turn on power to the disk drive.

10. Remove system data disk pack from drive.

11. Install a known good scratch pack into drive.

12. Push A or B port switch in (depends on port chosen in step 4 and the one that is now connected to the FTB).

13. Connect the FTB's line cord to the same ac power source as that of the drives.

14. Refer to Paragraph 4.4 for operating instructions.

4.4 FTB OPERATING INSTRUCTIONS

The cabling setup procedures outlined in Paragraph 4.3 must be performed before initializing the disk drive/FTB configuration. Once the cabling is complete, the operating procedures for exercising and testing the drive from the FTB are the same for both types of system.

NOTE
Steps 1 through 4 of the following procedure initializes both the drive and tester for test purposes.

1. Perform initial FTB test setup by setting the front panel controls as follows.

Control	Position
DRIVE TYPE	Up (RK07) for testing RK07 drive Down (RK06) for testing RK06 drive
EXERCISE/STATUS	EXERCISE
DRIVE SELECT	Same as drive under test

COMMAND TO RK06/7

DESELECT/RELEASE	To the left (negated)
SEEK	To the left (negated)
RECALIBRATE	To the left (negated)
START SPINDLE	To the left (negated)
RTC	To the left (negated)
CLEAR ERROR & ATTENTION	To the left (negated)
20/22 SECTORS	To the right (22)
SET MEDIUM OFF LINE	To the right (asserted)
SET VOLUME VALID	To the left (negated)

LOOP CONTROL

SINGLE CYCLE/CONTINUOUS	CONTINUOUS
FUNCTION	SEEK ONLY
SYNC	WR CLK
CLOCK	FAST
HALT ON ERROR	NO

ADDRESSING

CYLINDER	SWR
CYLINDER SWITCH REGISTER (2^0-2^9)	All down (negated)
HEAD	SWR
Head Switch Register (2^0-2^1)	Down (negated)
SECTOR	ZERO ONLY
MESSAGE A and B PARITY	ODD

2. Perform the following steps to start the disk drive from the drive's control panel.

   a. Press the STOP pushbutton on the tester.

   b. Press the drive's RUN/STOP to the RUN position. The spindle motor should start and when up to speed, the heads will load and stop on cylinder 0.

3. Perform the following steps to stop the disk dive from the tester.

> **NOTE**
> **The initial FTB setup outlined in step 1 is configured to stop the drive when the START pushbutton is asserted.**

   a. Press the START pushbutton on the tester. The carriage assembly will retract and unload the heads to the "home" position. The spindle motor will then come to a gradual stop.

4. Perform the following steps to start the disk drive from the tester.

   a. Set the following front panel controls on the tester as indicated.

Control	Position
START SPINDLE	To the right (asserted)
SET MEDIUM OFF LINE	To the left (negated)
SET VOLUME VALID	To the right (asserted)

   b. Press the START pushbutton on the tester. The spindle motor should start and when up to speed, the heads will load and stop on cylinder 0.

NOTE

Assertion of the tester's START/STOP pushbuttons will now start and stop tester operation. In order to stop the disk drive (unload heads etc.), the STOP pushbutton must be pressed (asserted) and the SET MEDIUM OFF LINE asserted (to the right), START SPINDLE negated (to the left), and SET VOLUME VALID negated (to the left), followed by START. Reverse the above procedure to start the drive (load heads etc).

5. If the drive to be tested is a known good drive, the basic loop mode can be used to exercise the drive. To initiate basic loop operation, perform the following steps.

   a. Press the STOP pushbutton on the tester.
   b. Set the FTB front panel controls to the following positions.

Control	Position
EXERCISE/STATUS	EXERCISE
DRIVE SELECT	Same as drive under test
COMMAND TO RK06/7	
DESELECT/RELEASE	To the left (negated)
SEEK	To the right (asserted)
RECALIBRATE	To the left (negated)
START SPINDLE	To the right (asserted)
RTC	To the left (negated)
CLEAR ERROR & ATTENTION	To the left (negated)
20/22 SECTORS	To the right (22)
SET MEDIUM OFF LINE	To the left (negated)
SET VOLUME VALID	To the right (asserted)

LOOP CONTROL

SINGLE CYCLE/CONTINUOUS	CONTINUOUS
FUNCTION	SEEK & W/R
SYNC	WR CLK
CLOCK	FAST
HALT ON ERROR	YES

ADDRESSING

CYLINDER	ALT (SWR SEQUENTIAL)
CYLINDER SWITCH REGISTER (2^0-2^9)	All down
HEAD	ALL
SECTOR	ALL
MESSAGE A and B PARITY	ODD

6. Press the START pushbutton on the tester. The disk drive should perform alternate seeks [ALT (SWR↔SEQUENTIAL)] and write/reads (SEEK and W/R) on all heads (ALL) and all sectors (ALL).

7. Observe MESSAGE A and MESSAGE B status LED for error indications. If any errors occur, the tester will halt operation [HALT ON ERROR (YES)].

8. If a Drive Fault occurs, set the EXERCISE/STATUS switch to the STATUS position and check each status message line using the MESSAGE SELECT switch. Refer to Appendix B for a detailed description of the status messages.

9. To stop the drive from the tester, press the STOP pushbutton and set the SET MEDIUM OFF LINE to the right (asserted), START SPINDLE to the left (negated), and SET VOLUME VALID to the left (negated). Press START on the tester. The heads will retract and the carriage assembly will move to the "home" position. The spindle will slow down and come to a gradual stop.

4.5 HEAD ALIGNMENT

The RK6/7 FTB contains functionally independent circuitry and hardware for performing read/write head alignment. The READ/WRITE signal is amplified and displayed on the dc microamperes meter on the FTB's control panel. This is similar to the manner in which the disk drive processes the tracks following servo signals.

4.5.1 Head Alignment Principles

There are several critical principles that must be understood before attempting head alignment. These principles make the head alignment procedure easier to understand and will help avoid damage or improper alignments of the heads. These principles are as follows.

1. Do not attempt to perform head alignment on a malfunctioning drive. The head alignment procedures are based on the assumption that the drive being aligned is a properly operating drive.

2. The drive's WRITE PROT switch should always be asserted (on) when an alignment pack is installed in the drive. As an additional precautionary measure, set the safety switch (S2) on module M7729 (on the RK06) or M7906 (on the RK07) to the MAINT position. This feature prevents the heads from unloading if a servo unsafe condition occurs during head alignment.

3. Do not apply more than minimum lateral force to the carriage when performing head alignment. Excessive force will cause damage to the heads, pack, and positioner.

4. The head alignment fixture and positioner parts are precision mechanical devices and must be handled carefully.

5. Use recommended tools and fixtures to ensure that critical alignments are secure and to avoid damage to the precision parts and fixtures.

6. Power up the disk drive and allow it to run for 2 hours before attempting head alignment.

7. Install the correct alignment pack (RK06K-AC for an RK06 drive, RK07K-AC for an RK07 drive) and allow it to rotate 1/2 hour prior to beginning head alignment.

8. The servo head is fixed and only the data heads are aligned.

4.5.2 Head Alignment (with FTB)

The following equipment is required.

- RK6/7 Field Test Box
- Head alignment fixture
- Torque wrench (adjustable) from 2 to 5 in-lb
- Hex bits (0.062 and 0.093 bits)
- RK06K-AC alignment cartridge (for aligning heads on an RK06)
- RK07K-AD alignment cartridge (for aligning heads on an RK07)

1. Refer to FTB operating procedures (Paragraph 4.4) for tester setup and operating procedures.

2. Stop the disk drive from the tester

   a. Press the FTB's STOP pushbutton.
   b. Set the SET MEDIUM OFF LINE switch to the right (asserted).
   c. Set the START SPINDLE switch to the left (negated).
   d. Set the SET VOLUME VALID switch to the left (negated).
   e. Press the FTB's START pushbutton.

3. After the drive spindle stops, remove the scratch pack and install an alignment pack.

4. Remove the rear cover from the disk drive and trip the main circuit breaker to the OFF position.

5. Pull the card cage open (out and downward) and set the safety switch (S2) on the M7729 (on an RK06) or M7906 (on an RK07) module to the MAINT position.

6. Press the WRITE PROTECT switch on the drive's control panel to the on position (asserted). This provides dual protection against accidently writing on the alignment pack.

7. Secure the read/write preamplifier (from FTB) to the drive's base casting using the Velco strips that are provided.

8. Connect the FTB's head alignment preamplifier plug into the drive's read/write pins. On early-model drives, an adapter is used to connect the head alignment cable to the read/write module along with a ground lead (Figure 4-4).

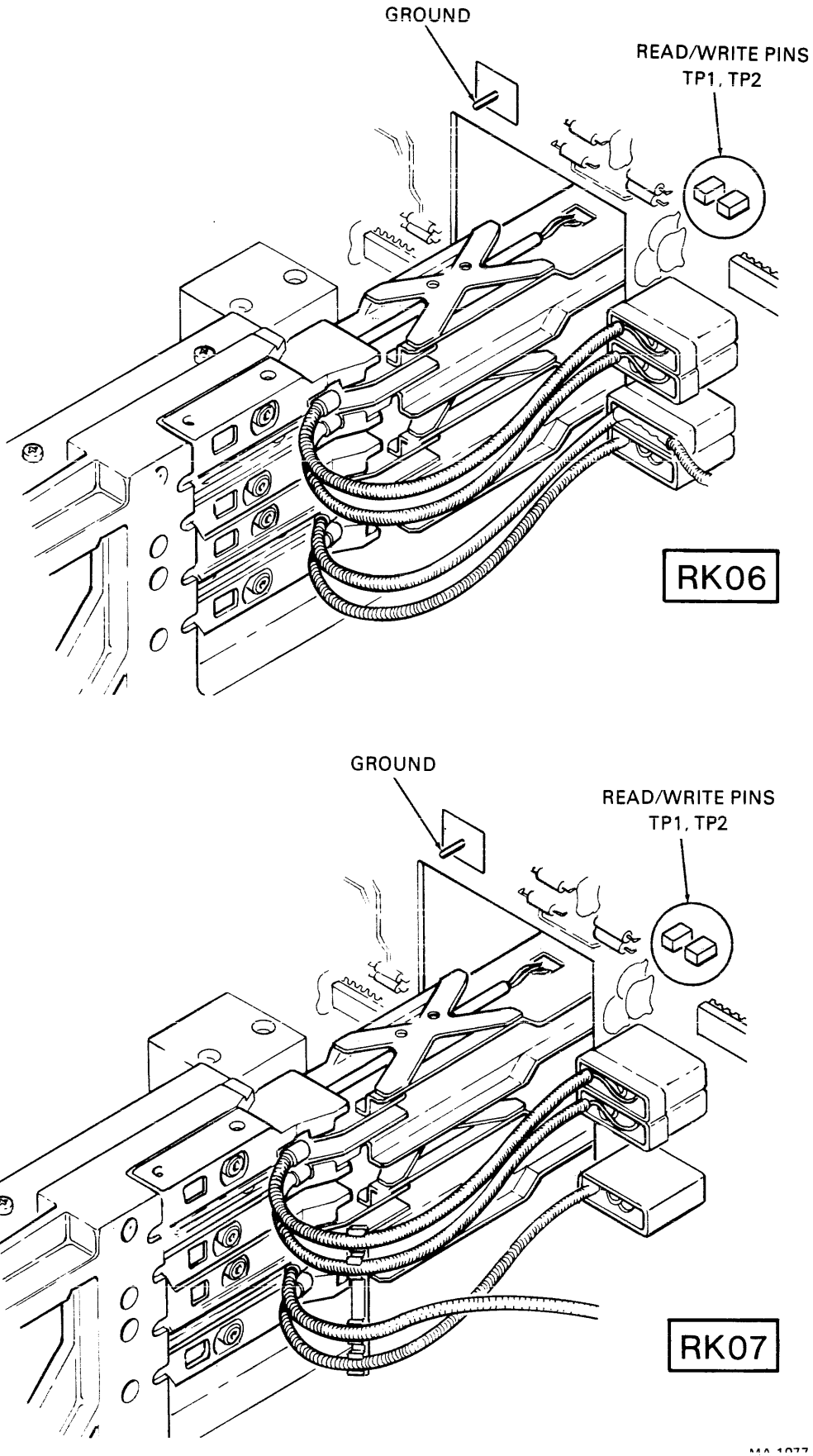


Figure 4-4 Read/Write Module Test Points

9. Set the following switches on the FTB.

Control	Position
EXERCISE/STATUS	EXERCISE
SINGLE CYCLE/CONTINUOUS	SINGLE CYCLE
LOOP FUNCTION	SEEK ONLY
SYNC	INT
CYLINDER ADDRESSING	SWR
CYLINDER SWITCH REGISTER (2^0-2^9)	All underlined switches up (asserted) for an RK06 All dotted switches up (asserted) for an RK07
HEAD	SWR
HEAD SWITCH REGISTER (2^0-2^1)	Down (i.e., head zero selected)

10. Set the main circuit breaker on the disk drive to the ON position.

11. Perform the following steps to start the disk drive from the tester.

    a. Set the START SPINDLE switch to the right (asserted).
    b. Set the SET MEDIUM OFF LINE switch to the left (negated).
    c. Set the SET VOLUME VALID switch to the right (asserted).

12. Press the START pushbutton on the tester. The spindle motor will start and come up to speed and the heads will load. The drive will do a single seek to cylinder 245 if the underlined cylinder switches were asserted (RK06 alignment), or to cylinder 496 if the dotted cylinder switches were asserted (RK07 alignment).

13. Check that the METER VALID LED lights and does not flash and the meter does not peg. Check that the appropriate drive type LED (to the left of the meter) is lit.

14. Read/write head 0 is now selected, since both head register switches are down (see Step 9).

15. Select head 1 by asserting switch 2^0 located under the HEAD SWR and pushing START. Check that the METER VALID LED lights and does not flash and the meter does not peg.

16. Select head 2 by asserting switch 2^1 and pushing START. Check that the METER VALID LED lights and does not flash and the meter does not peg.

17. If all read/write heads are within tolerance (i.e., 0 ± 10 μA (i.e., 0 ± 50 μ IN.)), the test is complete and no adjustments are necessary. However, if any (or all) heads fail to meet the recommended tolerance, they must be adjusted using the head alignment fixture.

18. Stop the disk drive from the tester.

    a. Press the FTB's STOP pushbutton.
    b. Set the SET MEDIUM OFF LINE switch to the right (asserted).
    c. Set the START SPINDLE switch to the left (negated).
    d. Set the VOLUME VALID switch to the left (negated).
    e. Press the FTB's START pushbutton. The carriage will retract to the home position and unload heads and the spindle will slow to a gradual stop.

19. If no alignments are necessary, remove the alignment pack and head alignment cables from the drive and return the drive to normal operation. If alignments are required, continue with the next step in this procedure.

20. With the read/write heads unloaded, install the head alignment fixture on the head needing alignment as illustrated in Figure 4-5.

NOTE

Turn both vertical adjustment screws fully counterclockwise (ccw) to facilitate installation of the fixture.

21. Using the torque wrench, tighten the head alignment fixture hex-head mounting screw to 5 in-lb. Loosen the read/write head set screw and torque it to 2 in-lb.

22. Perform the following steps to start the disk drive from the tester.

    a. Set the START SPINDLE switch to the right (asserted).
    b. Set the SET MEDIUM OFF LINE switch to the left (negated).
    c. Set the SET VOLUME VALID switch to the right (asserted).
    d. Set the head needing alignment in the HEAD SWR switches.

23. Press the FTB's START pushbutton. The drive will do a single seek to cylinder 245 (for an RK06 head alignment) or to cylinder 496 (for an RK07 head alignment).

24. To move the read/write head toward the spindle, adjust the forward vertical adjustment screw using the 5 in-lb torque wrench. To move the read/write head toward the carriage assembly, adjust the rear vertical adjustment screw using the 5 in-lb torque wrench.

NOTE

The head alignment fixture set screws operate on a ramp, fighting each other. Therefore, one of the set screws must always be in the fully counterclockwise (ccw) position to ensure proper adjustment.

25. Adjust the head alignment set screws until the head alignment meter indicates 0 ± 10 μA and the METER VALID LED glows steadily. or 0 ± 50μIN.

26. Adjust is complete when both vertical adjustment screws are loose (no forward or reverse tension) and the head alignment meter indicates 0 ± 10 μA.
or 0 ± 50μIN.

27. Perform the following steps to stop the disk drive.

    a. Press the STOP pushbutton on the tester.
    b. SET MEDIUM OFF LINE switch to the right (asserted).
    c. Set the START SPINDLE switch to the left (negated).
    d. Set the SET VOLUME VALID switch to the left (negated).
    e. Press the FTB's START pushbutton.

28. Tighten the head set screw to 5 in-lb.

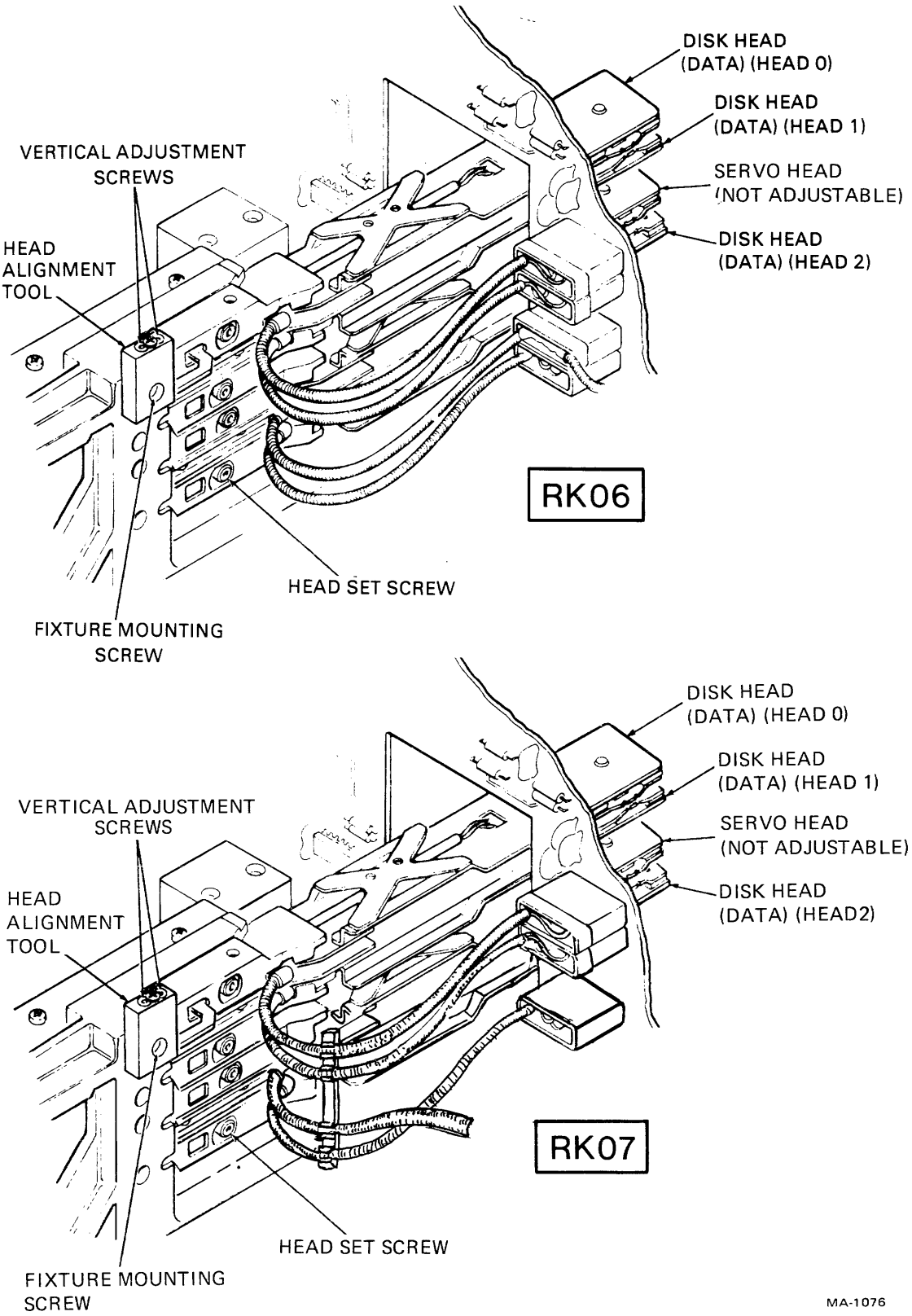


Figure 4-5 Read/Write Heads and Alignment Fixture

29. Perform the following steps to start the disk drive.

    a. Set the START SPINDLE switch to the right (asserted).
    b. Set the SET MEDIUM OFF LINE switch to the left (negated).
    c. Set the SET VOLUME VALID switch to the right (asserted).
    d. Press the FTB's START pushbutton

30. Check the head alignment meter to ensure that head alignment adjustments are within the specified tolerances. If adjustments fail, repeat steps 25 through 30.

31. Stop the disk drive (see step 27) and remove the head alignment fixture.

32. Repeat steps 20 through 31 and verify alignment for read/write heads 1 and 2.

33. When the alignments are complete, stop the disk drive and the tester and remove the alignment pack.

34. Set the safety switch (S2) on the M7729 (on an RK06 drive) or M7906 (on an RK07 drive) servo module to the normal position and deselect the WRITE PROT switch on the drive's control panel.

35. Remove the head alignment cable and preamplifier from the disk drive.

36. Return disk drive to system configuration.

4.5.3 Head Alignment (Program Control)

The following equipment is required for RK06 or RK07 drive head alignment via program control.

- Head alignment program (MAINDEC 11-DZR6N)
- RK6/7 Field Test Box (FTB)
- Head alignment fixture
- Torque wrench (adjustable) 2 and 5 in-lb
- Hex bits (0.093 and 0.062 bits)
- RK06K-AC alignment cartridge (for aligning heads on an RK06)
- RK07K-AC alignment cartridge (for aligning heads on an RK07)

1. Press the drive's RUN/STOP pushbutton to the STOP position.

2. Remove the rear cover from the drive unit and trip the main circuit breaker to the OFF position.

CAUTION

Ensure power is removed (OFF) from both the FTB and the disk drive before attaching the alignment cable to the read/write board.

3. Pull the card cage open (out and downward) and set the safety switch (S2) on the M7729 (on an RK06 drive) or M7906 (on an RK07 drive) servo module to the MAINT position.

4. Press the WRITE PROTECT switch on the drive's front panel to the on position (asserted). This provides dual protection against accidentally writing on the alignment pack.

5. Secure the read/write preamplifier (from FTB) to the drive's base casting using the Velcro strips that are provided.

6. Connect the FTB's head alignment preamplifier plug into the drive's read/write pins that are available for this purpose. On early model drives, an adapter is used to connect the head alignment cable to the read/write module along with a ground lead (Figure 4-4).

7. Set the main circuit breaker on the disk drive to the on position.

8. Connect the FTB to ac power source (same as drive's, if possible) and turn the tester ON.

9. Load MAINDEC-11-DZR6N into the computer and start at address 224 (Figure 4-6).

10. Install the alignment pack into the disk drive (per program instructions).

11. Respond to program printout as illustrated in the sample program printout (Figure 4-6).

    a. MANUAL OR AUTO MODE (M or A)? = A
    b. ENTER DRIVE NO. (0–7): = 0
    c. ALIGN, VERIFY, OR EXERCISE (A, V, or E)? = A
    d. ENTER HEAD NO. (0–2): = 0
    e. TYPE R WHEN READY: = R

12. Check that the carriage does a single seek and that the program printout indicates that the heads are at cylinder 365 octal (RK06) or 760 octal (RK07).

13. Verify that the METER VALID LED lights and does not flash and that the meter does not peg.

14. Repeat step 13 for head 1 and 2. (i.e., 0 ± 50 μIN.)

15. If all read/write heads are within tolerance (i.e., 0 ± 10 μA), the test is complete and no adjustments are necessary. However, if any (or all) heads fail to meet the recommended tolerance, they must be adjusted using the head alignment fixture.

16. If no alignments are necessary, type <↑c> to exit the program and set the driver's RUN/STOP pushbutton to the STOP position. Remove the alignment pack and head alignment cables from the drive and return the drive to normal operation.

    If adjustments are required, continue with the next step in this procedure.

17. Type <↑c> to exit the program. The carriage will retract to the home position and unload the heads.

18. Set the drive's RUN/STOP pushbutton to the STOP position.

19. With the read/write heads unload, install the head alignment fixture as illustrated in Figure 4-5.

20. Using the torque wrench, tighten the head alignment fixture hex-head mounting screw to 5 in-lb.

21. Loosen the read/write head set screw and torque it to 2 in-lb.

22. Set the drive's RUN/STOP pushbutton to the RUN position and load the MAINDEC-11-DZR6N as outlined in step 11.

```
DZR6N-D - RK611/RK06-RK07 SUBSYSTEM VERIFICATION : PART 2


*** RK06-07 HEAD ALIGNMENT AID ***
FOR HELP TYPE H, ELSE CR
H
INSTRUCTIONS FOR USING RK06-RK07 HEAD ALIGNMENT AID :
**************************************************
MOUNT AN RK06 OR RK07 ALIGNMENT CARTRIDGE ON THE DESIRED
DRIVE, AND INSURE THAT THE DRIVE IS WRITE-LOCKED.
CONNECT THE ALIGNMENT INDICATOR TO THE DESIRED DRIVE,
VIA THE HEAD ALIGNMENT CABLE ONLY, AND CYCLE UP THE
DRIVE. AFTER MOUNTING THE PACK ON THE DRIVE,
THE OPERATOR SHOULD WAIT 30 MINUTES FOR THE DRIVE
TEMPERATURE TO STABILIZE, BEFORE PROCEEDING WITH
ALIGNMENT.

RESPOND TO ALL REQUESTS FOR PARAMETERS, BY ENTERING
THE DESIRED PARAMETER VALUE (NO <CR> NEEDED).
THERE ARE TWO MODES OF OPERATION : MANUAL MODE
ALLOWS SELECTION OF DRIVES AND HEADS BY TTY INPUT,
AND AUTO MODE ALLOWS DRIVES AND HEADS TO BE SELECTED
BY OFF-ON OPERATION OF DRIVE PORT SELECT SWITCHES.
IN EITHER MODE, UP TO 5 MINUTES OF SEEK EXERCISES
MAY BE REQUESTED FOR EACH DRIVE.
ALSO IN EITHER MODE, A VERIFY OPERATION ALLOWS HEAD
SELECTION WITHOUT THE UNLOADING AND LOADING OF
THE DRIVE BY THE PROGRAM, WHICH OTHERWISE OCCURS
TO ALLOW MANIPULATION OF THE ALIGNMENT TOOL.
TO RESTART EITHER MODE, TYPE ^Z .
TO RESTART ALIGNMENT AID, TYPE ^R .
TO SELECT NEW DRIVES IN MANUAL MODE, TYPE ^C .

FOR HEAD ALIGNMENT PROCEDURE, REFER TO FIELD
TEST BOX (RK06-07TA, RK06-07TB) OPERATOR'S MANUAL.

MANUAL OR AUTO MODE (M OR A)?
M


* MANUAL SELECT MODE *

ENTER DRIVE NO. (0-7):
0
DRIVE SER. NO.  ?

ALIGN, VERIFY OR EXERCISE (A, V, OR E)?
A
```

Figure 4-6 Sample Program Printout (Sheet 1 of 2)

```
* MANUAL SELECT ALIGNMENT *

ENTER HEAD NO. (0-2)
0
TYPE <R> WHEN READY:
R
HEADS POSITIONED AT CYLINDER 365 (OCT)
HEAD 0 SELECTED

ENTER HEAD NO. (0-2) :
1
TYPE <R> WHEN READY:
R
HEADS POSITIONED AT CYLINDER 365 (OCT)
HEAD 1 SELECTED

ENTER HEAD NO. (0-2) :
2
TYPE <R> WHEN READY:
R
HEADS POSITIONED AT CYLINDER 365 (OCT)
HEAD 2 SELECTED

ENTER HEAD NO. (0-2) :
^Z

ALIGN, VERIFY, OR EXERCISE (A, V, OR E) ?
E
TYPE <R> WHEN READY
R


*RANDOM SEEK EXERCISES IN PROGRESS ON DRIVE 0
^Z

ALIGN, VERIFY, OR EXERCISE (A, V, OR E) ?
V


* MANUAL SELECT VERIFY *

ENTER HEAD NO. (0-2) :
2
HEADS POSITIONED AT CYLINDER 365 (OCT)
HEAD 2 SELECTED

ENTER HEAD NO. (0-2) :
^Z
```

Figure 4-6 Sample Program Printout (Sheet 2 of 2)

0±50μIN.

23. Adjust the head alignment set screws until the head alignment meter indicates 0 ± 10 μA and the METER VALID LED glows steadily. Tighten the read/write head set screw to 5 in-lb.

24. Repeat 17 through 23 for heads 1 and 2.

25. When adjustments are complete, type <↑c> to exit the program. Set the drive's RUN/STOP pushbutton to STOP position.

26. Remove the head alignment fixture.

27. Repeat steps 9 through 15 to ensure that alignment is within specifications.

28. When alignments and verifications are complete, stop the disk drive and remove the alignment pack and head alignment cables.

29. Set the safety switch (S2) on the RK06 M7729 or RK07 M7906 servo module to the normal position and deselect the WRITE PROT switch on the front panel of the drive.

30. Return the drive to the system configuration.

CHAPTER 5
MAINTENANCE

5.1 SCOPE

This chapter provides a complete description to aid service personnel in isolating and repairing faults in the FTB circuitry and components. There are no recommended preventive maintenance steps; however, both visual and operational checks should be performed at periodic intervals to ensure proper operation.

5.2 OFF-LINE TEST PROCEDURE

The off-line test procedure is intended to demonstrate that the FTB circuitry, front panel controls, and indicators are functioning properly.

NOTE

In performing the series of tests that follow, UNLESS OTHERWISE STATED, the DRIVE TYPE switch on the tester must be left in the RK07 position. Toward the end of the series of tests, a few special tests will be performed to ascertain the proper functioning of the sections of the tester that are unique to the testing of an RK06 drive.

The following steps and procedures are designed to thoroughly checkout the FTB for any malfunctions.

1. Open suitcase cover and remove the tester from carrying case.
2. Remove all modules from the card cage.
3. Place the tester on a convenient working surface.
4. Attach the power supply cable and attach the LOAD BOARD.
5. Connect the ac power cord to a wall receptacle.
6. Check for the following voltages.

+5 V	+15 V	-5 V	-15 V
A1A2	D1D2	D1R1	D1B2
A2A2	D3D2	B3F2	C4B2
A3A2	A4D2	D3F2	
A4A2	C4D2	A4R2	

7. Remove the ac power cord from the wall receptacle.

8. Remove the LOAD BOARD and attach the power supply extension cable from the power supply to the backplane connector.

9. Replace modules in the slots as indicated (Figure 5-1), with the control module (G5256) on a quad extender and the transceiver module (G5166) on a dual extender.

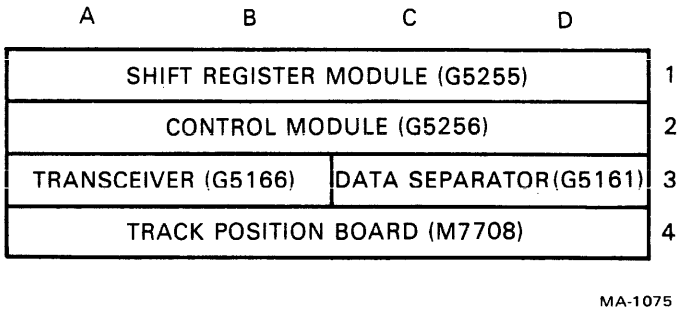


Figure 5-1 Field Test Box Module Utilization

10. Check the resistance of voltage pins to ground and to each other.

Voltage Pin	Resistance Level
+5 V +15 V -5 V -15 V	Between 0Ω and 10 KΩ

11. Connect the power extension cable to the backplane connector.

12. Replace the ac power cord in the wall receptacle.

13. Check the clock frequency on the data separator board (G5161) by attaching an oscilloscope probe to D3J2 and observing that eight clock periods equal 116.25 ns × 8 = 930 ns. If this is not the case, adjust potentiometer R15 on this board.

14. Put the switches on the front panel to the positions indicated.

EXERCISE/STATUS to EXERCISE
DRIVE SELECT to proper position
COMMAND TO RK06/7 switches:
DESELECT to the left position (negated)
SEEK to the left position (negated)
RECALIBRATE to the left position (negated)
RTC to the left position (negated)
CLEAR ERROR & ATTENTION to the left position (negated)
20/22 SECTORS to the right position (22 SECTORS)
SET MEDIUM OFF LINE to the left position (negated)
SET VOLUME VALID to the left position (negated)

LOOP CONTROL switches:
SINGLE CYCLE/CONTINUOUS to CONTINUOUS
FUNCTION to SEEK ONLY
SYNC to INT
CLOCK to FAST
HALT ON ERROR to NO
ADDRESSING switches:
CYLINDER to SWR
HEAD to SWR
SECTOR to ZERO ONLY
SWITCH REGISTER – all switches down (negated)

15. Push the START button and then the STOP button. All 32 of the LEDs in MESSAGE words A and B should be OFF.

16. Take a chip clip and, on the shift register module (G5255), jumper E40-13 to E40-7 (ground). This makes the tester receive all 1s in MESSAGE words A and B. In the A message word, the READY bit is always asserted to allow the tester to increment the cylinder address counter.

NOTE
For the remainder of this test procedure (off-line testing), whenever the tester is to be started, first push the STOP button and then push the START button.

17. Start the tester and then stop it. All the A and B MESSAGE LEDs should be ON. If not, check the LEDs that are off and see that they have approximately 3 V on the anodes. The cathodes should all be common and at ground potential. If these conditions are met and any LEDs are not on, replace them. If the anode of an LED is at ground, then look for a fault on the shift register module (G5255). DRIVE FAULT and DATA OR PARITY ERROR should be on, dimly, when the tester is started.

18. Disconnect the jumper to E40-13 but leave E40-11 connected to E40-7.

19. Start the tester.

20. Enable HEAD SWR 2^0 and 2^1 and ensure that the LED above each switch comes on when the switch is enabled.

21. Enable CYLINDER ADDRESS SWITCHES 2^0 to 2^9 sequentially and ensure that all corresponding LEDs come on. As the ADDRESS switches are enabled, the T4–T13 LEDs in MESSAGE B should come on dimly, with the following relationship:

CYL SWR:	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9
MSG B LED:	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13

22. Transmit MESSAGE A to drive.

    a. Put probe No. 1 on E17-2 on the shift register module (G5255), and put probe No. 2 on E25-9 (CTD-H) of the same module. Sync on the leading edge.

    b. Ensure that the MESSAGE A switches are all down (negated).

c. Enable the MESSAGE A switches, one at a time, and check the parity for each one before disabling it.

d. When checking bit 0, STROBE XMIT should be asserted. Check this at E1-17 on the control module (G5256).

e. As successive bits are asserted, the STROBE XMIT H pulse should appear in successive positions on the oscilloscope, whereas CTD H should be high for a total length of 17 bits (Figure 5-2).

f. Put CLOCK switch in SLOW position. CTD-H (at E25-9) should be approximately 7.8 μs × 64 = 500 μs. After checking time, put CLOCK back to FAST.

g. Table 5-1 indicates the meaning of the bits T0 through T15.

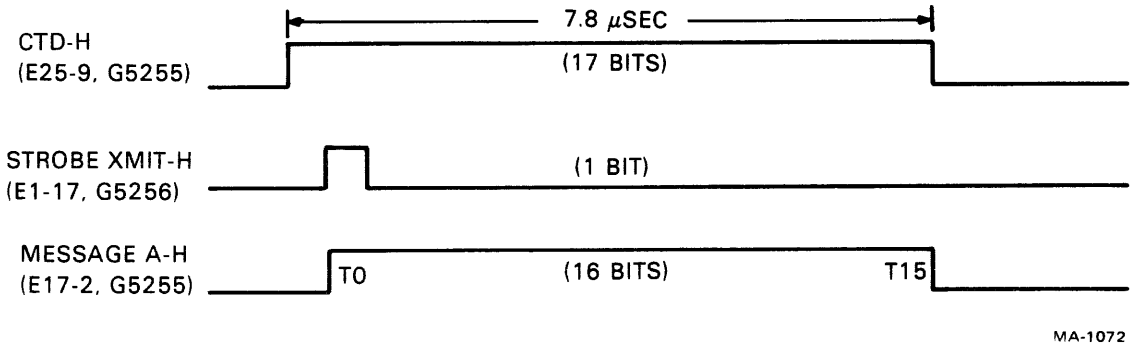


Figure 5-2 Timing Diagram, Transmission of MESSAGE A to Drive

23. Transmit MESSAGE B to drive. Bits T0 through T15 are checked in a manner similar to that in Step 22.

a. Place these switches as indicated.

COMMAND TO RK06/7 switches:
DESELECT/RELEASE to the left (negated)
SEEK to the left (negated)
RECALIBRATE to the left (negated)
START SPINDLE to the left (negated)
RTC to the left (negated)
CLEAR ERROR & ATTENTION to the left (negated)
20/22 SECTORS to the right (22 SECTORS)
SET MEDIUM OFF LINE to the left (negated)
SET VOLUME VALID to the left (negated)
SWR switches - all down (negated)

b. Move probe No. 1 and chip clip at E17-2 to E33-2, but leave sync probe No. 2 at E25-9 (CTD-H).

c. Ensure that MESSAGE B switches are all down (negated).

Table 5-1 Definition of MESSAGE A Bits T0 to T15

Bit	Meaning
T0	DRV SELECT 1H when BCD switch asserted
T1	DRV SELECT 2H when BCD switch asserted
T2	DRV SELECT 4H when BCD switch asserted

Bits T0 through T2 are asserted in this order:

BCD Switch DRV SEL CODE	Bit T0	Bit T1	Bit T2
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1

T3	DESEL RELEASE H when switch asserted
T4	SEEK H when switch asserted
T5	RECALIBRATE H when switch asserted
T6	START SPINDLE H when switch asserted
T7	RTC H when switch asserted
T8	CLR ERR AND ATTENTION H when switch asserted
T9	FORMAT 20 SECTOR when switch asserted
T10	SET MEDIUM OFF LINE H when switch asserted
T11	SET VOLUME VALID H when switch asserted
T12	2^0 HEAD H when asserted (HEAD switch up)
T13	2^1 HEAD H when asserted
T14	LOGIC 0 ALWAYS
T15	PARITY SWITCH in ODD position: T15 is H if T0 – T14 contain an even number of 1s T15 is L if T0 – T14 contain an odd number of 1s PARITY SWITCH in EVEN position: T15 is H if T0 – T14 contain an odd number of 1s T15 is L if T0 – T14 contain an even number of 1s

d. Enable the MESSAGE B switches, one at a time, and check the parity for each one before disabling it.

e. When checking bit 0, STROBE XMIT should be asserted. Check this at E1-17 on the control module (G5256).

f. As successive bits are asserted, the STROBE XMIT H pulse should appear in successive positions on the oscilloscope, whereas CTD H should be high for a total length of 17 bits (Figure 5-3).

g. Enable STATUS switch in the upper left-hand corner of the front panel. In the STATUS mode, the tester will cycle once and come to a halt, so the intensity of the oscilloscope screen will have to be turned up to see if bits T0 and T1 are asserted.

h. The MESSAGE SELECT switch is located on the lower left section of the front panel. Table 5-2 shows the coding of this switch. Check to see that bits T0 and T1 are correct.

i. Put the EXERCISE/STATUS switch back to the EXERCISE mode and turn down the intensity of the oscilloscope, because the tester will now cycle continuously.

The next set of steps checks the operaton of the tester with MESSAGE A IN asserted and B IN negated.

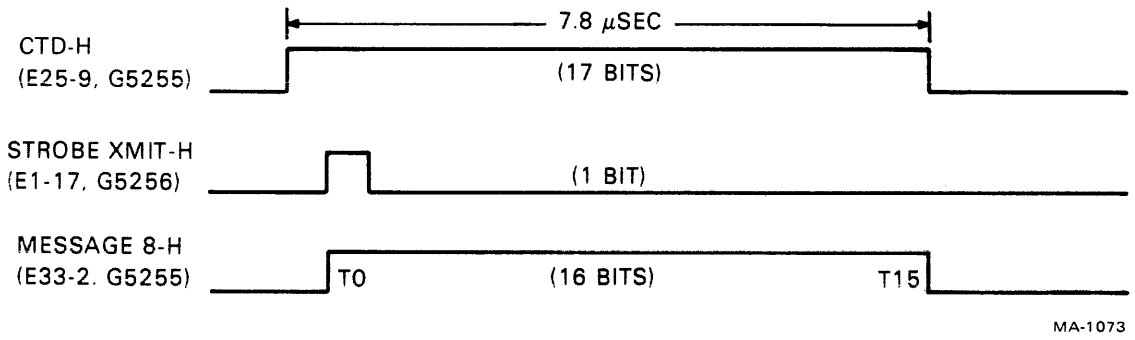


Figure 5-3 Timing Diagram, Transmission of MESSAGE B to Drive

24. Adjust the switches as follows:

SINGLE CYCLE/CONTINUOUS to SINGLE CYCLE
CYLINDER to SWR
SWR switches all DOWN
HALT ON ERROR to NO
CLOCK to FAST
SYNC to INT
HEAD to ALL
DELAY potentiometer should be adjusted for ease of viewing LEDs in the following tests

25. Loop Control Test: Single Cycle Mode – In this mode, when START is pushed, the tester formulates a message and transmits it to the drive repetitively until the drive responds with DRIVE READY. The tester then increments itself and halts.

NOTE

No individual test will be performed specifically on this feature. However, it will be used in the following addressing tests, and any misoperation of this feature will cause failure of the test. Do not push STOP after START, because this will initialize the tester and all counter information will be cleared.

Table 5-2 Definition of MESSAGE B Bits T0 to T15

Bit	Meaning	MESSAGE SELECT Switch
T0	ST WRD 0	0 Position (00)
T1	ST WRD 1	1 Position (01)
T2	Logic 0 always	2 Position (10)
T3	Logic 0 always	3 Position (11)
T4	H when 1 in the SWR is asserted	
T5	H when 2 in the SWR is asserted	
T6	H when 4 in the SWR is asserted	
T7	H when 8 in the SWR is asserted	
T8	H when 16 in the SWR is asserted	
T9	H when 32 in the SWR is asserted	
T10	H when 64 in the SWR is asserted	
T11	H when 128 in the SWR is asserted	
T12	H when 256 in the SWR is asserted	
T13	H when 512 in the SWR is asserted	
T14	Logic 0 always	
T15	PARITY SWITCH in ODD position: T15 is H if T0 – T14 contain an even number of 1s T15 is L if T0 – T14 contain an odd number of 1s PARITY SWITCH in EVEN position: T15 is H if T0 – T14 contain an odd number of 1s T15 is L if T0 – T14 contain an even number of 1s	

26. Head Switch Test – The head counter is a 2-bit modulo three counter that is enabled with the switch in the ALL position. It increments every cycle time and sequentially selects heads in this manner: 0, 1, 2, 0, 1, 2, 0, 1, . . .

Table 5-3 is a chart of the head counter operation. Push START and check that the counter increments once every time START is pushed. The SINGLE CYCLE/CONTINUOUS switch should be on SINGLE CYCLE.

Table 5-3 Head Counter Operation (Modulo 3)

Selected Head	2^1	2^0
0	0	0
1	0	1
2	1	0
0	0	0

After checking, put SINGLE CYCLE/CONTINUOUS back to CONTINUOUS mode. Put the HEAD switch back to SWR position and the HEAD SWR switches in the down position.

27. Oscillation Test - Put CYLINDER switch into the OSC mode. A 10-bit latch is loaded by the CYLINDER SWR switches and 0 alternately. Put the 2^9 switch (512) in the up position. Start tester and see if LEDs alternate between the two modes.

28. Sequential Test - Put CYLINDER switch in SEQUENTIAL mode. A 10-bit latch is loaded by the contents of a 10-bit binary counter located on the G5255 shift register module. When the tester is started, this 10-bit counter should reset to 0 and start incrementing until the count of 814 is reached, then it will reset to 0 and start counting over again (Table 5-4). To check the counter at 814, wait until 512 (2^9), 256 (2^8), and 32 (2^5) are asserted. Then put SINGLE CYCLE/CONTINUOUS to SINGLE CYCLE, and push START until the count of 814 is reached and resets to 0.

Table 5-4 Reset of Sequential Address Count (RK07)

	512 2^9	256 2^8	128 2^7	64 2^6	32 2^5	16 2^4	8 2^3	4 2^2	2 2^1	1 2^0
Count of 814	1	1	0	0	1	0	1	1	1	0
Next Count	0	0	0	0	0	0	0	0	0	0

Put the HEAD switch to the ALL position and manually push START and see that when 2^1 in the HEAD counter is reached, the next count increments the 10-bit binary counter and the head counter goes to 0.

29. Alternate Mode Test - Put CYLINDER switch to ALT mode. Table 5-5 shows how the cylinder address and head counters sequence with the SINGLE CYCLE/CONTINUOUS switch in SINGLE CYCLE mode. Assert the 2^9 bit of the cylinder SWR.

    In this mode, the cylinder address switch alternates between SEQUENTIAL and SWR mode. The 10-bit counter in the SEQUENTIAL mode is incremented once by the HEAD counter after 2^1 is reached, which, in turn, toggles flip-flop E15-5 to the SWR mode. The head counter resets to 0, counts to 2^1, and toggles E15 to the SEQUENTIAL mode but does not increment the binary counter.

Table 5-5 Cylinder Address and Head Count Sequencing

Cylinder Address Mode	10-Bit Binary Counter 2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Head Count 2^1	2^2
SWR	1	0	0	0	0	0	0	0	0	0	0	0
SWR	1	0	0	0	0	0	0	0	0	0	0	1
SWR	1	0	0	0	0	0	0	0	0	0	1	0
SEQUENTIAL	0	0	0	0	0	0	0	0	0	0	0	0
SEQUENTIAL	0	0	0	0	0	0	0	0	0	0	0	1
SEQUENTIAL	0	0	0	0	0	0	0	0	0	0	1	0
SWR	1	0	0	0	0	0	0	0	0	0	0	0
SWR	1	0	0	0	0	0	0	0	0	0	0	1
SWR	1	0	0	0	0	0	0	0	0	0	1	0
SEQUENTIAL	0	0	0	0	0	0	0	0	0	1	0	0
SEQUENTIAL	0	0	0	0	0	0	0	0	0	1	0	1
SEQUENTIAL	0	0	0	0	0	0	0	0	0	1	1	0
SWR	1	0	0	0	0	0	0	0	0	0	0	0
SWR	1	0	0	0	0	0	0	0	0	0	0	1
SWR	1	0	0	0	0	0	0	0	0	0	1	0
SEQUENTIAL	0	0	0	0	0	0	0	0	1	0	0	0
SEQUENTIAL	0	0	0	0	0	0	0	0	1	0	0	1
SEQUENTIAL	0	0	0	0	0	0	0	0	1	0	1	0
SWR	1	0	0	0	0	0	0	0	0	0	0	0

Put SINGLE CYCLE/CONTINUOUS back to CONTINUOUS and start the tester.

30. FTB in RK06 Mode - Two of the tests described previously, with the tester in the RK07 mode, must be repeated with the tester in the RK06 mode.

    a. Oscillation Test - With DRIVE TYPE set to RK06, put the CYLINDER addressing switch to OSC. Put the 2^9 and 2^8 cylinder SWR switches up. Start the tester. Only the 2^8 LED should light because the tester is in the RK06 mode.

    b. Sequential Test - With DRIVE TYPE set to RK06, put the CYLINDER addressing switch to SEQUENTIAL. The 10-bit latch is loaded by the contents of the 10-bit binary counter. When the tester is started, the 10-bit counter should reset to 0 and start incrementing until the count of 410 is reached. It will reset to 0 and start counting over again. To check the counter at 410, wait until 256 (2^8) and 128 (2^7) are asserted. Then, put SINGLE CYCLE/CONTINUOUS to SINGLE CYCLE and push the START button until the count of 410 is reached and resets to 0, as shown in Table 5-6.

Table 5-6 Reset of Sequential Address Count (RK06)

	512 2^9	256 2^8	128 2^7	64 2^6	32 2^5	16 2^4	8 2^3	4 2^2	2 2^1	1 2^0
Count of 410	0	1	1	0	0	1	1	0	1	0
Next Count	0	0	0	0	0	0	0	0	0	0

    c. After the completion of both of these tests, return the DRIVE TYPE switch to RK07.

31. DELAY KNOB Test – This variable control delays the READY signal asserted from the drive for approximately 220 μs to 0.7 seconds. Move probe No. 2, which is at E33-2, to E33-9 (DISPLAY-L). The time between DISPLAY-L pulses, when DISPLAY-L is negated, should vary as the DELAY knob is rotated. DISPLAY-L is the sum of CTD-H and RCV-H signals. Vary the knob over the entire range. It should be a smooth transition (Figure 5-4).

32. HALT ON ERROR Switch Test – Place switch in YES position. Note that the LED counter halts immediately and the DATA/D to C PARITY ERROR LED comes on. It halts because all 1s are going into MESSAGE A. Sixteen 1s is EVEN PARITY, which is an error condition because MESSAGE A and MESSAGE B are always sent with ODD PARITY.

33. Set the tester up for on-line testing.

    a. Take chip clips off the shift register module.

    b. Disconnect the jumper from E40-11 to E47-7.

    c. Hook up the 40 conductor flat cable (BC06R-2) to the transceiver board (G5166), making sure that the red stripe is at Pin 1 of the connector on the board. The other end of the cable goes to the I/O connector on the front panel. Make sure that Pin 1 agrees with the connector.

    d. Leave the control module on the extender, for use in the on-line testing.

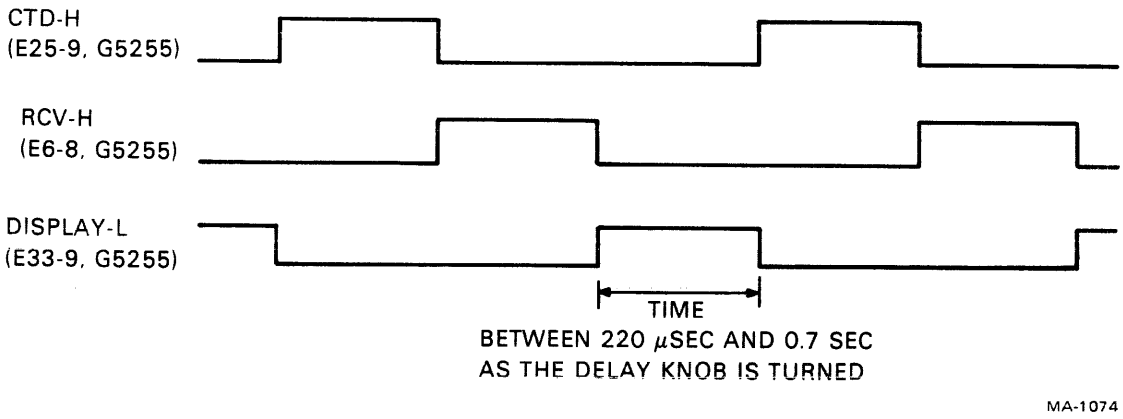


Figure 5-4 Timing Diagram, Delay of DISPLAY-L

5.3 ON-LINE TEST PROCEDURE

The on-line test procedure is intended to demonstrate that the FTB is functioning properly. If it is possible that the FTB is malfunctioning, the off-line test procedure described in Paragraph 5.2 should be performed and successfully completed before attempting any on-line checks.

NOTE
It is necessary that the drive used in the on-line testing is known to be functioning properly.

1. Connect one end of the drive I/O cable to J1A in the drive connector, and connect the other end to the tester I/O connector.

2. Connect terminator to J2A on the drive connector block.

3. Check that the RUN/STOP switch on the front of the drive is in the OUT position (negated).

4. Turn on the breaker on the rear of the drive and check that the drive spindle motor does not turn on.

5. Insert a known good scratch pack (not an alignment pack) into the drive. Use only an RK06K-DC cartridge in an RK06 drive, and only an RK07K-DC cartridge in an RK07 drive.

6. Ensure that the M7706 module is in slot 3 of the drive card cage.

7. Push the drive's PORT A button in.

8. Place the DRIVE TYPE switch on the tester to RK07. Make sure that the RK07 LED immediately to the left of the alignment meter is on and that the RK06 LED is off.

9. Place these switches in the indicated positions:

   EXERCISE/STATUS to EXERCISE

   DRIVE SELECT switch - to match the number on the drive's UNIT SELECT plug (on the front of the drive)

   COMMAND TO RK06/7 switches:
   DESELECT/RELEASE to the left position (negated)
   SEEK to the left position (negated)
   RECALIBRATE to the left position (negated)
   START SPINDLE to the left position (negated)
   CLEAR ERROR & ATTENTION to the left position (negated)
   RTC to the left position (negated)
   20/22 SECTORS to the right position (22 SECTORS)
   SET MEDIUM OFF LINE to the right position (asserted)
   SET VOLUME VALID to the left position (negated)

   LOOP CONTROL switches:
   SINGLE CYCLE/CONTINUOUS to CONTINUOUS
   FUNCTION to SEEK ONLY
   SYNC to WR CLK
   CLOCK to FAST
   HALT ON ERROR to NO

   ADDRESSING switches:
   CYLINDER to SWR
   SWR - all 10 switches down (negated)
   HEAD to SWR
   HEAD SWR - both switches down (negated)
   SECTOR to ZERO ONLY
   MESSAGE A PARITY to the ODD position
   MESSAGE B PARITY to the ODD position

10. Push STOP button on tester.

11. Push RUN/STOP switch (on the drive) in. The drive spindle should start up and, when it is up to speed, the carriage assembly should load the heads and stop at cylinder 0.

12. Start the tester. The tester switches are set to stop the drive. Note that the heads unload and the spindle motor slows, then stops.

13. Stop the tester.

14. Place the COMMAND TO RK06/7 switches as indicated:

    DESELECT to the left position (negated)
    SEEK to the left position (negated)
    RECALIBRATE to the left position (negated)
    START SPINDLE to the right position (asserted)
    CLEAR ERROR & ATTENTION to the left position (negated)
    RTC to the left position (negated)
    20/22 SECTOR to the left position (20 SECTORS)
    SET MEDIUM OFF LINE to the left position (negated)
    VOLUME VALID to the right position (asserted)

15. Start the tester. The drive spindle motor should start and then the heads will load.

16. Stop the tester.

17. Place the DESELECT/RELEASE switch to the right (asserted) position, and the SINGLE CYCLE/CONTINUOUS switch to SINGLE CYCLE.

18. Check that the SACK LED is on.

19. Start the tester.

20. Check that the SACK LED goes off and that the DATA/D to C PARITY ERROR LED goes on.

21. Stop the tester.

22. Put the DESELECT/RELEASE switch to the left position.

23. Start the tester.

24. Check that the SACK LED goes on and that the PARITY OR DATA ERROR LED goes off. The SACK assertion from the drive shows that it has received a message from the tester and is selected.

25. Check that the POLLED ATTENTION LED is on.

26. Stop the tester. Place the tester switches as indicated in Step 9.

27. Start the tester. This will stop the drive.

28. Start the drive by repeating Steps 13, 14, and 15.

    Before the drive can assert the POLLED ATTENTION line, two conditions have to be satisfied in the drive. The STATUS CHANGE flip-flop has to be set and the number on the three POLLED ADDRESS LINES from the tester's transceiver board has to agree with the drive number. The number on these POLLED ADDRESS LINES is derived from the tester DRIVE SELECT SWITCH.

29. Stop the tester.

30. Place the SINGLE CYCLE/CONTINUOUS switch to SINGLE CYCLE and the MESSAGE B PARITY switch to EVEN.

31. Start the tester. The DRIVE FAULT LED should go on.

32. Put the CLEAR ERROR & ATTENTION switch to the right position and put the MESSAGE B PARITY switch to ODD.

33. Press START and check that the DRIVE FAULT LED goes off.

34. Place these switches as indicated:

    CLEAR ERROR & ATTENTION to the left position
    SEEK COMMAND to the right position
    HALT ON ERROR to YES
    MESSAGE A PARITY to EVEN

35. Start the tester. These LEDs should come on:

    DRIVE FAULT
    POLLED ATTENTION
    SACK

36. Place MESSAGE A PARITY to ODD.

37. Push CONTROLLER POWER OFF. The DRIVE FAULT LED should be on and the POLLED ATTENTION and SACK LEDs should be off.

38. Start the tester. The DRIVE FAULT, POLLED ATTENTION, and SACK LEDs should be off.

39. Push the INITIALIZE button. Check that SACK and POLLED ATTENTION go off and that DRIVE FAULT remains on.

40. Start the tester. Check that DRIVE FAULT goes off and that POLLED ATTENTION and SACK go on.

41. Push the MULTIPLE DRIVE SELECT pushbutton. The tester asserts the SECTOR AND INDEX line, which normally can only be asserted by a drive. The drive being tested detects sector and index pulses that are not its own and shuts down. Check that the heads retract to the home position and that the MULTIPLE DRIVE SELECT LED goes on.

42. Check that the POLLED ATTENTION, SACK, and DRIVE FAULT LEDs are all on.

43. Place these switches as indicated:

    HALT ON ERROR to NO
    CYLINDER ADDRESS - SWR mode, 2^7 (128) asserted
    CLEAR ERROR & ATTENTION to the right (asserted)
    SINGLE CYCLE/CONTINUOUS to SINGLE CYCLE
    SEEK to the right (asserted)
    FUNCTION to SEEK ONLY

44. Start the drive by repeating Steps 13, 14, and 15. After the drive is up to speed, the heads should load (to cylinder 0) and then seek to cylinder 128.

45. Check that the following are on:

    SACK LED
    POLLED ATTENTION LED
    READY light (on front of drive)
    MESSAGE A bit T7

46. Place the switches as indicated:

    LOOP CONTROL switches:
    SINGLE CYCLE/CONTINUOUS to SINGLE CYCLE
    FUNCTION to SEEK ONLY
    HALT ON ERROR to NO
    CLOCK to FAST
    SYNC to WR CLK

    DELAY potentiometer should be adjusted for ease of viewing LEDs in the following tests

    ADDRESSING switches:
    CYLINDER to SWR
    SWR - all switches down (negated)
    HEAD to ALL

47. Loop Control Test - In the SINGLE CYCLE mode, when START is pushed, the tester formulates a message and transmits it to the drive repetitively until the drive responds with DRIVE READY. The tester then increments itself and halts.

> **NOTE**
> **No individual test will be performed specifically on this feature. However, it will be used in the following addressing tests, and any misoperation of this feature will cause failure of the test. Do not push STOP after START, because this will initialize the tester and all counter information will be cleared.**

48. Head Switch Test - The head counter is a 2-bit modulo three counter that is enabled with the head switch in the ALL position. It increments every cycle time and sequentially selects heads in this manner: 0, 1, 2, 0, 1, 2, 0, 1, . . .

    Table 5-7 is a chart of the head counter operation. Push the START button and check that the counter increments once every time START is pushed. SINGLE CYCLE/CONTINUOUS should be on SINGLE CYCLE.

Table 5-7 Head Counter Operation (Modulo 3)

Selected Head	2^1	2^0
0	0	0
1	0	1
2	1	0
ŭ	ŭ	ŭ

49. Put HEAD switch to the SWR position and put all the HEAD SWR switches in the down position.

50. Cylinder Address Test – Put the CYLINDER switch (under ADDRESSING) to the SWR mode. The 10-bit cylinder latch and 2-bit head latch located on the shift register module (G5255) are loaded with the contents of the cylinder and head address registers when the tester is started. To test, enable the 2^0 bit in the CYLINDER ADDRESS SWR, push START, and check that the 2^0 LED and only the 2^0 LED comes on.

    Disable the 2^0 switch and enable the 2^1 switch. Push START and check that the 2^1 LED and only the 2^1 LED comes on. Continue this process until all ten switches and their respective LEDs have been tested. Every time the START switch is pushed, the drive should have performed a seek to the address in the SWR.

51. Oscillation Test – Put the CYLINDER switch (under ADDRESSING) to the OSC position. The 10-bit latch on G5255 is loaded with the contents of the SWR switches and zero, alternately. Put the 2^9 CYLINDER switch in the up position. Push START several times in succession and check that the LEDs and the carriage assembly of the drive alternate between 512 (2^9) and 0.

52. Sequential Test (Part 1) – Put the CYLINDER switch in the SEQUENTIAL mode. A 10-bit latch is loaded by the contents of a 10-bit binary counter located on the shift register module. When the tester is started, this 10-bit counter should reset to 0 and start incrementing until the count of 814 is reached. Then, it will reset to 0 and start counting over again. To check the counter at 814, wait until 512 (2^9), 256 (2^8), and 32 (2^5) are asserted. Then, put SINGLE CYCLE/CONTINUOUS to SINGLE CYCLE, and push the START button until the count of 814 is reached and resets to 0. Table 5-8 shows the coding for a count of 814 and then a count of 0.

Table 5-8 Reset of Sequential Address Count (RK07)

	512 2^9	**256** 2^8	**128** 2^7	**64** 2^6	**32** 2^5	**16** 2^4	**8** 2^3	**4** 2^2	**2** 2^1	**1** 2^0
Count of 814	1	1	0	0	1	0	1	1	1	0
Next Count	0	0	0	0	0	0	0	0	0	0

Sequential Test (Part 2) – Put the DRIVE TYPE switch to RK06 mode. Put SINGLE CYCLE/CONTINUOUS to CONTINUOUS and the CYLINDER switch to the SEQUENTIAL mode. The 10-bit latch on G5255 will be loaded with the contents of a 10-bit binary counter located on the shift register module. Stop the tester, then press START.

When the tester is started, the 10-bit counter should reset to 0, start incrementing until the count of 410 is reached, and then reset to 0 and start counting over again. To check the counter at 410, wait until 256 (2^8) and 128 (2^7) are asserted, then put SINGLE CYCLE/CONTINUOUS to SINGLE CYCLE. Push the START button, repetitively, until the count of 410 is reached. The next time START is pushed, the count will go to 0 (Table 5-9).

Table 5-9 Reset of Sequential Address Count (RK06)

	512 2^9	256 2^8	128 2^7	64 2^6	32 2^5	16 2^4	8 2^3	4 2^2	2 2^1	1 2^0
Count of 410	0	1	1	0	0	1	1	0	1	0
Next Count	0	0	0	0	0	0	0	0	0	0

Put the HEAD switch to the ALL position. Push STOP and then, repetitively, push START and check that when 2^1 in the HEAD counter is reached that the next count increments the 10-bit binary counter and the head counter goes to 0 per Table 5-10.

Table 5-10 SWR Display and Head Count

SWR								HEAD Switch – ALL Position Head Counter			
2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^1	2^0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	1	0	1	0
0	0	0	0	0	0	0	0	1	1	0	0

53. Put DRIVE TYPE switch back to RK07 mode and put the CYLINDER switch to the HALT position.

54. Alternate Mode Test – In this mode, the cylinder address latch is loaded alternately from the sequential counter and the SWR switches. The 10-bit sequential counter is incremented once by the head counter after 2^1 is reached, which, in turn, toggles flip-flop E15-5 to the SWR mode. The head counter resets to 0 and then counts to 2^1 and toggles E15 to the sequential mode but does not increment the binary counter.

Table 5-11 shows how the CYLINDER ADDRESS and HEAD COUNTERS sequence with the tester in SINGLE CYCLE operation. Push STOP, and then START, and check that the tester CYLINDER and HEAD LEDs appear as in Table 5-11.

Table 5-11 Cylinder Address and Head Count Sequencing

Cylinder Address Mode	10-Bit Binary Counter 2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Head Count 2^1	2^0
SWR	1	0	0	0	0	0	0	0	0	0	0	0
SWR	1	0	0	0	0	0	0	0	0	0	0	1
SWR	1	0	0	0	0	0	0	0	0	0	1	0
SEQUENTIAL	0	0	0	0	0	0	0	0	0	0	0	0
SEQUENTIAL	0	0	0	0	0	0	0	0	0	0	0	1
SEQUENTIAL	0	0	0	0	0	0	0	0	0	0	1	0
SWR	1	0	0	0	0	0	0	0	0	0	0	0
SWR	1	0	0	0	0	0	0	0	0	0	0	1
SWR	1	0	0	0	0	0	0	0	0	0	1	0
SEQUENTIAL	0	0	0	0	0	0	0	0	0	1	0	0
SEQUENTIAL	0	0	0	0	0	0	0	0	0	1	0	1
SEQUENTIAL	0	0	0	0	0	0	0	0	0	1	1	0
SWR	1	0	0	0	0	0	0	0	0	0	0	0
SWR	1	0	0	0	0	0	0	0	0	0	0	1
SWR	1	0	0	0	0	0	0	0	0	0	1	0
SEQUENTIAL	0	0	0	0	0	0	0	0	1	0	0	0
SEQUENTIAL	0	0	0	0	0	0	0	0	1	0	0	1
SEQUENTIAL	0	0	0	0	0	0	0	0	1	0	1	0
SWR	1	0	0	0	0	0	0	0	0	0	0	1

55. Stop the tester.

56. Place the switches in the indicated positions:

    20/22 SECTORS to the right (22 SECTORS)
    LOOP CONTROL switches:
    SINGLE CYCLE/CONTINUOUS to CONTINUOUS
    FUNCTION to WRITE
    HALT ON ERROR to NO
    ADDRESSING switches:
    CYLINDER to SWR
    512 (in SWR) up (asserted)
    all other SWR switches down (negated)
    HEAD to SWR
    SECTOR to ZERO ONLY

57. Sync Switch Test – Put the SYNC switch to the WR CLK position. Take probe No. 1 and go to backplane pin C2K1 of tester (PPL DATA DRIVE-L) and check that there are clock transitions. Put SYNC switch to the INT position and check that the clock transitions stop. Put SYNC switch back to WR CLK position.

    Start the tester and check that the drive seeks to cylinder 512. Take a chip clip, go to the G5256 module, to E15-3, with probe No. 1, and use it to sync on the leading edge of INDEX-L. Take probe No. 2, go to E15-11, SECTOR-L, and count the number of SECTOR pulses between INDEX pulses. There must be 22 sector pulses corresponding with the COMMAND TO RK06/7 switch for 22 SECTOR format. Stop the tester and change to 20 SECTOR format. Start the tester and check that there are 20 sector pulses between index pulses.

Figure 5-5 shows timing diagrams to correspond with the following procedure and explanation.

Take probe No. 2, go to E9-6 (WRITE GATE-L) on the G5256 module and check that the signal is low just for sector 0 time (the SECTOR switch is in the ZERO ONLY position). Put the SECTOR switch to the ALL position and check that the WRITE GATE-L signal is low for each and every sector. Check that between sectors, WRITE GATE-L is high for approximately 1 μs. The reason is that WRITE GATE cannot be asserted as SECTOR-L trailing edge time or the drive will get a drive error (READ/WRITE UNSAFE). Check with probe No. 2 that one shot E13-12 on the G5256 module is approximately 0.8 μs wide and located as shown in Figure 5-5. Take probe No. 2, go to E28-12 (WRITE DATA-H) on module G5256. Check that sector 0 and all other even sectors have a high frequency signal of 232 ns/cycle and all odd sectors have a low frequency of 434 ns/cycle. Put the SINGLE CYCLE/CONTINUOUS switch to SINGLE CYCLE.

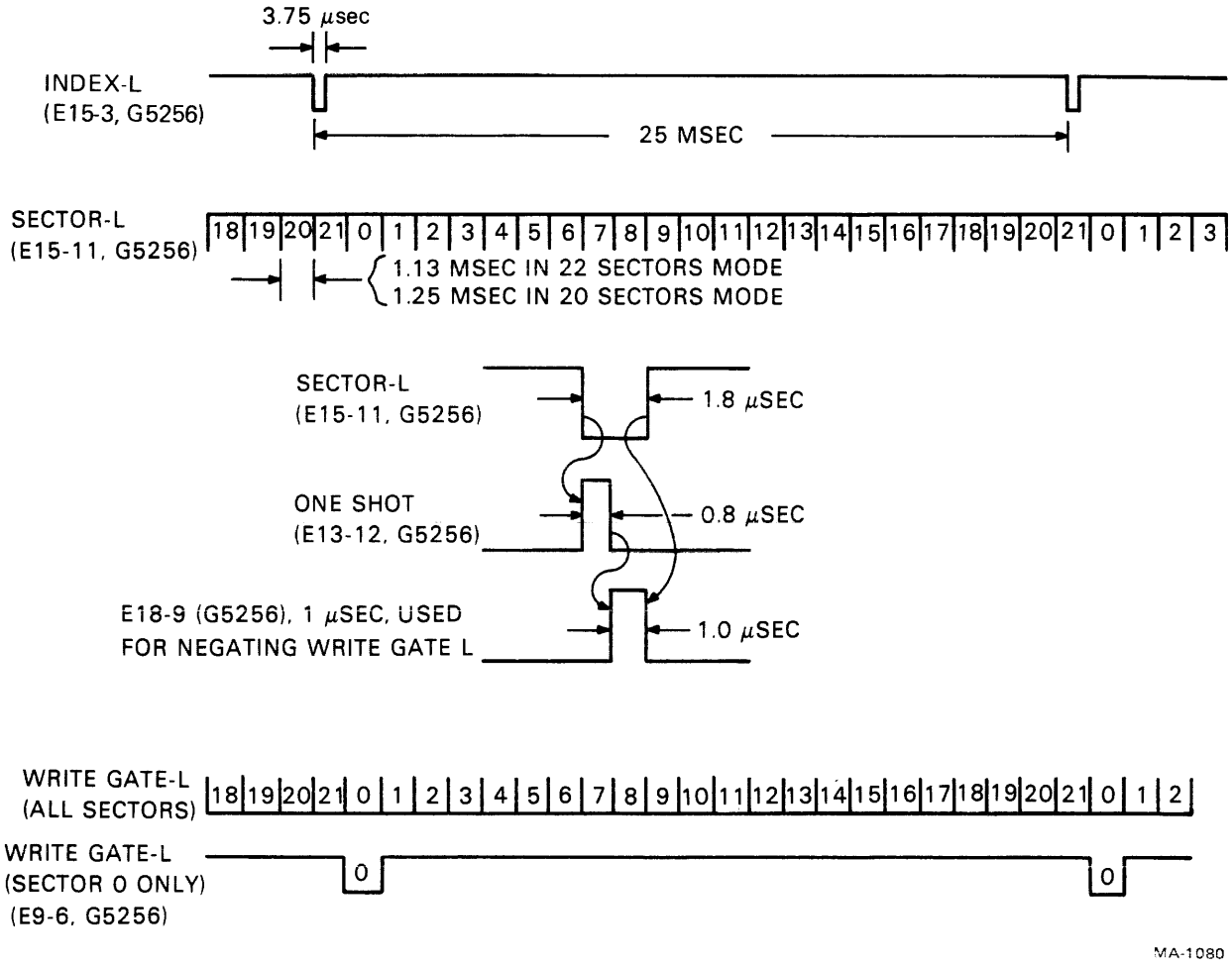


Figure 5-5 Timing Diagram, WRITE GATE-L

58. Seek/Read Test – Place these switches as indicated.
LOOP CONTROL switches:
SINGLE CYCLE/CONTINUOUS to CONTINUOUS
FUNCTION to SEEK & READ
HALT ON ERROR to NO

20/22 SECTORS to the left (20 SECTORS)
SECTOR to ALL

Figure 5-6 gives a timing diagram to accompany the following discussion.

Start the tester and take probe No. 2 to E28-8 (READ GATE-H) on the G5256 module. READ GATE-H should be asserted for each and every sector. Between sectors, check that READ GATE-H is low for approximately 50 μs. This 50 μs is a one-shot that is triggered by the leading going edge of SECTOR-L. The reason for the delay in reading is that the phase-locked loop in the tester data separator module (G5156) must have time to lock to the written data so that it will decode data correctly. Put the SECTOR switch to ZERO ONLY. Check that READ GATE-H is asserted only for sector 0.

Take probe No. 2 and go to E21-1. This is READ DATA-L from the drive. Check that sector 0 and all even sectors have the high frequency of 232 ns/cycle and sector 1 and all odd sectors have the low frequency of 464 ns/cycle.

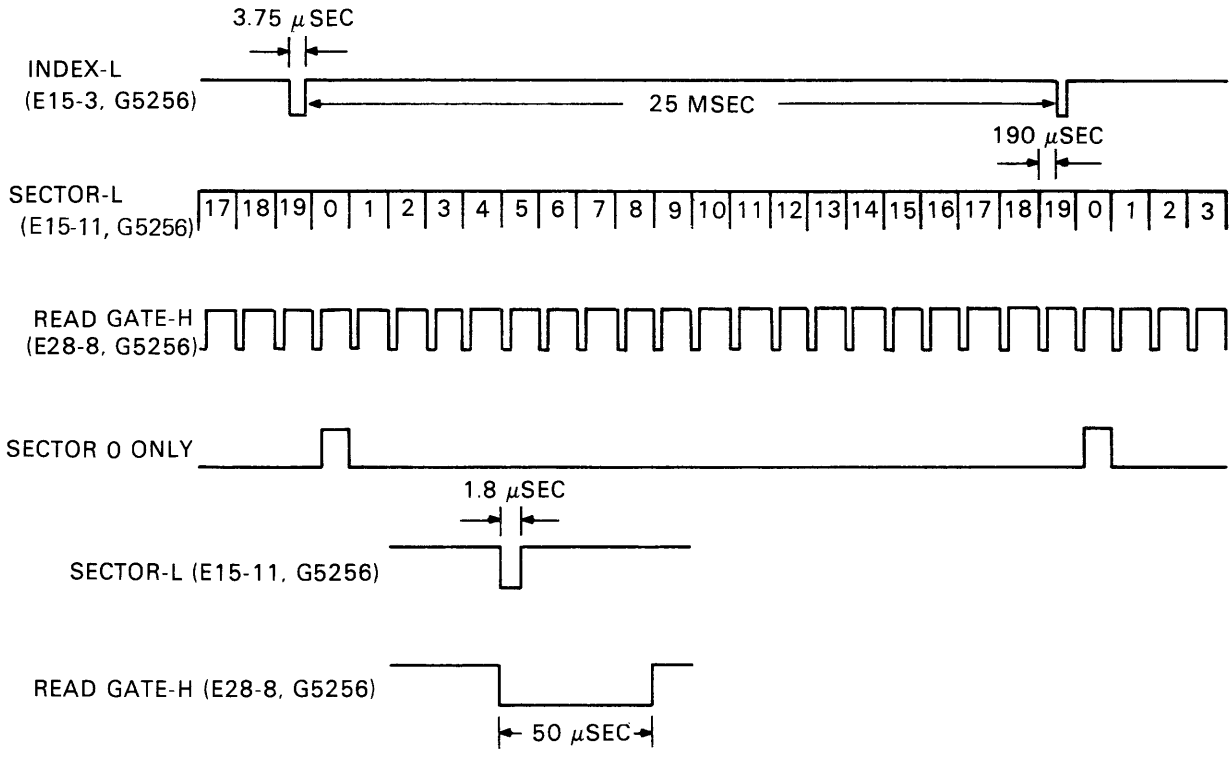


Figure 5-6 Timing Diagram, READ GATE-H

59. Read Error Detection Test - Put HALT ON ERROR in the YES position. The tester must continue reading data with no errors. Stop the tester. Put the SECTOR switch to ALL and the 20/22 SECTORS from 20 sectors to 22 sectors. Start the tester and check to see that the drive immediately comes to a halt with the DATA/D to C PARITY ERROR LED coming on. The reason is that the data was written in the 20 sector format, and it is being read in the 22 sector format, and the 20 sector mode sector pulse areas appear as read error areas in the 22 sector mode.

60. Seek/Write and Read Error Detection Test - Place these switches as shown:

    FUNCTION to SEEK & W/R
    HALT ON ERROR to YES
    CYLINDER to SEQUENTIAL
    HEAD to ALL

    Start the tester and let it sequence through all 814 cylinders several times and check that there are no data errors. If there are consistent errors, check the tester data separator module (G5161).

61. Read/Write Inhibit Test - Place these switches as shown:

    LOOP CONTROL switches:
    SINGLE CYCLE/CONTINUOUS to CONTINUOUS
    FUNCTION to SEEK & W/R
    HALT ON ERROR to YES
    ADDRESSING switches:
    CYLINDER to SWR
    HEAD to ALL

    Put 256, 128, 16, 8, and 2 cylinder switches in the asserted (up) position. Start the tester. Put a finger on the head selector diodes on the read/write module in the drive. They are situated just to the right of the read/write connectors on the read/write module. This action will generate errors in the drive. If the tester continuously runs and does not halt on any errors this means that, in the RK06 mode, read and write functions are inhibited and the artificially generated errors are not being detected. This is the expected result. Put the DRIVE TYPE switch back into the RK07 mode.

5.4 HEAD ALIGNMENT METER CHECK

The following steps are designed to functionally check the head alignment section of the tester box.

NOTE

This procedure is not intended to check the accuracy of the head alignment section since the validation is accomplished at the factory.

1. Ensure that the DRIVE TYPE switch is in the RK07 position.
2. Push the RUN/STOP switch on the drive to stop the drive.
3. Wait until the drive stops, then remove the scratch pack.
4. Open the drive card cage, if it is not already open.

5. Place the safety switch (S2) on the M7906 servo analog module to the MAINT position (toward the rear of the drive). This switch is the closer switch to the carriage assembly; it enables WRITE PROT on the front panel of the drive and disables the servo brake.

6. Check that the WRITE PROT light is on, then press the button.

7. Install an RK07K-AC alignment pack into the RK07 drive.

8. Attach the tester alignment preamp to the Velcro strips on the base casting of the drive. Plug the preamp into the RK07 read/write board alignment pins (Figure 4-4).

9. Place the tester switches as indicated.

   EXERCISE/STATUS to EXERCISE
   LOOP CONTROL switches:
   SINGLE CYCLE/CONTINUOUS to SINGLE CYCLE
   FUNCTION to SEEK ONLY
   SYNC to INT (for all alignment reading)

   ADDRESSING switches:
   CYLINDER to SWR
   HEAD to SWR
   HEAD SWR switches - both down (i.e., head zero is selected)
   Assert the dotted switches: 256, 128, 64, 32, and 16. This addresses cylinder 496 where the servo information is written.

10. Press the RUN/STOP switch on the drive.

11. Start the tester. Check that the drive does one seek to cylinder 496 and that the LED above the alignment meter is on but *not* flashing.

12. Select head 0 by negating 2^0 and 2^1 in HEAD SWR.

13. Start the tester. Observe that the ALIGNMENT VALID LED is on and that the meter is steady and not pegged.

14. Repeat Steps 12 and 13 for heads 1 and 2. Select head 1 by asserting only 2^0 in HEAD SWR; select head 2 by asserting only 2^1.

15. Pick the head with the best alignment reading (i.e., the smallest meter reading) and set the HEAD SWR switches for that head.

16. Offset Function Test - Set SEEK to the left position (negated), SINGLE CYCLE/CONTINUOUS to SINGLE CYCLE, and all CYLINDER SWR switches in the up position.

    When 256 and 128 are up and SEEK is negated, the drive goes into the offset mode. The 2^6 bit (64) is the polarity of the offset.

NOTE

The alignment meter's microamp to microinch conversion is "5" for the RK07 mode (as indicated by the RK07 alignment LED).

Table 5-12 shows some of the offsets and their corresponding codes. Put the CYLINDER SWR switches in the positions indicated in the table, pushing START after each new line is loaded. Check that the meter moves about the indicated amount in the indicated direction from the nominal setting.

Table 5-12 Typical Offsets

2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Meter Movement for RK07 Mode
1	1	1	1	1	1	1	1	1	0 μin
1	1	1	1	1	1	1	1	0	+12.5 μin to the left
1	1	1	1	1	1	1	0	1	+25.0 μin to the left
1	1	1	1	1	1	0	1	1	+50.0 μin to the left
1	1	1	1	1	0	1	1	1	+100.0 μin to the left
1	1	0	1	1	1	1	1	0	-12.5 μin to the right
1	1	0	1	1	1	1	0	1	-25.0 μin to the right
1	1	0	1	1	1	0	1	1	-50.0 μin to the right
1	1	0	1	1	0	1	1	1	-100.0 μin to the right

NOTE
The polarity of meter movements for the RK07 is opposite that for the RK06.

17. Final Preparation of Drive and Tester – After the alignment test has been completed, shut the drive down, from the tester. Remove the alignment pack from the drive, put S2 on the M7906 servo analog module back to the normal position (RUN), and disengage the WRITE PROT switch on the front of the drive. Stop the tester. Shut off ac power to the tester and remove the I/O cable from the drive and tester. Remove the card extender in slot No. 2 and put the control module (G5256) back into slot No. 2 in the tester. Put the module retainer (74-67503) back into place on the card cage and secure it to the cage.

APPENDIX A
FTB-TO-DRIVE MESSAGES

A.1 MESSAGE LINE A

This is a bidirectional signal line that transmits drive selection, commands, and head select data in serial form in a 16-bit format from the tester. At the time of drive selection determination, all other drives are inhibited from receiving the remainder of the transmission. Data from the selected drive to FTB on MESSAGE LINE A transmits status information via the MESSAGE A and MESSAGE B lines and displays them in the 16-bit message LEDs on the tester's front panel.

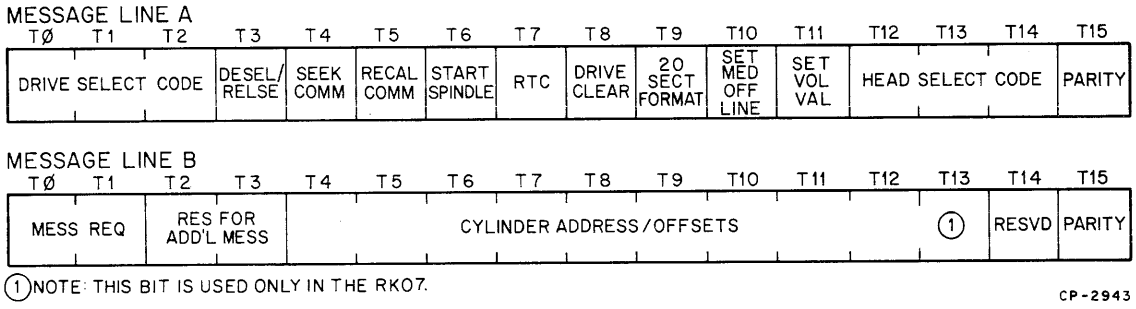


Figure A-1 MESSAGE LINE A FTB-to-Drive

Clock Period	Command	Description
T0 - T2	Drive Select Code	A 3-bit drive select code transmitted with the least significant bit first. All other drives are deselected.
T3	Deselect/Release	This command sets the drive available status to the other controller in a dual-access configuration. The drive is also deselected when this bit is asserted.
T4	Seek	This command directs the drive to seek to the cylinder address transmitted on MESSAGE LINE B.
T5	Recalibrate	This command directs the drive to seek to cylinder number 0 and to reset the cylinder address register. This command is used to resynchronize the drive position with its electronics if, for any reason, the two get out of step.

Clock Period	Command	Description
T6	Start Spindle	This command directs the drive to start spindle and, subsequently, to perform a brush cycle and load heads if, and only if, the RUN/STOP switch on the drive's front panel is depressed. It may also be used to restart a drive in the event that a set medium off-line command has unloaded heads or any of the error conditions that unload heads have occurred. However, the error must be cleared before this command will allow the heads to reload.
T7	Return to Centerline (RTC)	This command is used for resetting head offsets whenever a write operation is to take place. Clearing the offset mode requires 3 ms to complete, at which time a DRIVE ATTENTION signal is transmitted to the FTB. An RTC is implied by any non-zero cylinder seek or upon detection of a write gate in the event that an RTC command is not detected.
T8	Drive Clear	This bit, when asserted, clears the drive status change flip-flop as well as clearing all error flags in the selected drive (provided that the errors no longer exist).
T9	20-Sector Format Select	This bit, when asserted, commands 20-sectorpulses per disk rotation; when not asserted, 22-sector pulses are commanded. Twenty sectors correspond to 18-bit data words; 22 sectors correspond to 16-bit data words. Whenever a change in the format is made with this select bit, sector pulses cease, until the next sector 0 at which time the drive is synchronized to the new format.
T10	Set Medium Off Line	This bit, when asserted, unloads the drive heads and stops the spindle.
T11	Set Volume Valid	This bit, when asserted, sets the volume valid flip-flop, thereby acknowledging a power turn-on, a change of cartridge, or the removal of the unit select plug. This must be set in order to perform a write or seek function.
T12 - T13	Head Select Code	A 2-bit head select code (in binary-encoded form) is transmitted at these clock times with the LSB first. The seek command bit must be asserted in order to load the head addresses.
T14	Third Head Select Bit	This head select bit is reserved; it is always a logical 0.
T15	Parity	The state of this bit will be such that the number of logic 1s in the 16-bit transmission is odd.

A.2 MESSAGE LINE B

This bidirectional line transmits cylinder addresses, offset commands, and status message requests from the FTB to drive. When a drive is selected, all other drives will be inhibited from receiving the remainder of the transmission. Data transmitted from a selected drive to FTB on this line consists of various drive status messages in any of four MESSAGE B LEDs as requested from the FTB.

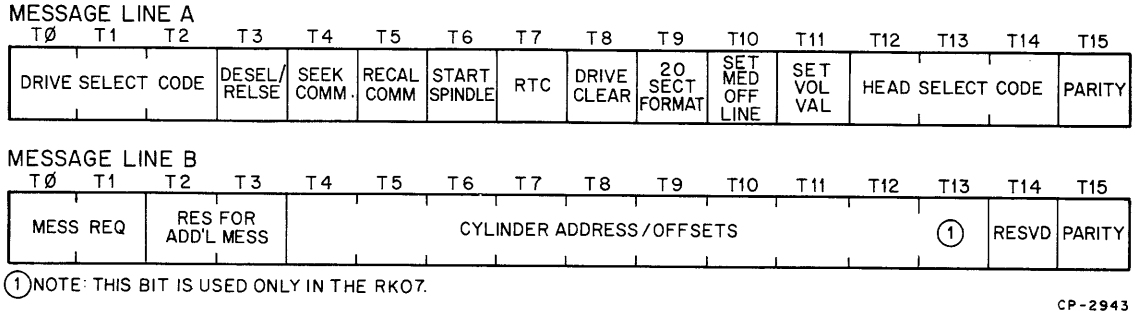


Figure A-2 MESSAGE LINE B FTB-to-Drive

Clock Period	Command	Description
T0 - T1	Message Request	When CTD is asserted, the state of these two-bits establishes which of the four sets of status messages (MESSAGE A or MESSAGE B) are transmitted from the selected drive to the FTB. T0 represents the least significant bit.
T2 - T3	Reserved	Reserved for additional message request bits.
T4 - T13	Cylinder Address/Offset Command	These data bits (all ten are used on the RK07, but only nine, T4 - T12, are used on the RK06) represent, when a seek command is asserted on MESSAGE LINE A, the desired cylinder address with the least significant bit transmitted first in binary form. When the seek command and recalibrate bits are low on MESSAGE LINE A and MESSAGE LINE B is true at T11 and T12 time, an offset command is generated with these bits. The codes for the different offsets are presented in Table A-3.

NOTE

A seek, RTC command, or recalibrate will clear the offset condition. Additionally, ready will be reset until the offset seek or the clearing of the offset condition is completed. Furthermore, a write gate received, when offset is on, causes a drive off-track error and fault.

Clock Period	Command	Description
T14	Reserved	Not Used.
T15	Parity	Parity bit for this 16-bit transmission.

Command T12	Command T11	Direction* T10	Magnitude T9	T8	T7	T6	T5	T4	Pin Offset Value (microinches) RK06	RK07
1	1	0/1	1	1	1	1	1	1	0	0
1	1	0/1	1	1	1	1	1	0	± 25	± 12.5
1	1	0/1	1	1	1	1	0	1	± 50	± 25.0
1	1	0/1	1	1	1	1	0	0	± 75	± 37.5
1	1	0/1	1	1	1	0	1	1	± 100	± 50.0
1	1	0/1	1	1	1	0	1	0	± 125	± 62.5
1	1	0/1	1	1	1	0	0	1	± 150	± 75.0
1	1	0/1	1	1	1	0	0	0	± 175	± 87.5
1	1	0/1	1	1	0	1	1	1	± 200	±100.0
1	1	0/1	1	1	0	1	1	0	± 225	±122.5
1	1	0/1	1	1	0	1	0	1	± 250	±125.5
1	1	0/1	1	1	0	1	0	0	± 275	±137.5
1	1	0/1	1	1	0	0	1	1	± 300	±150.0
1	1	0/1	1	1	0	0	1	0	± 325	±162.5
1	1	0/1	1	1	0	0	0	1	± 350	±175.0
1	1	0/1	1	1	0	0	0	0	±375	±187.5
1	1	0/1	1	0	1	1	1	1	± 400	±200.0
1	1	0/1	1	0	1	1	1	0	±425	±212.5
1	1	0/1	1	0	1	1	0	1	± 450	±225.0
1	1	0/1	1	0	1	1	0	0	±475	±237.5
1	1	0/1	1	0	1	0	1	1	± 500	±250.0
1	1	0/1	1	0	1	0	1	0	±525	±262.5
1	1	0/1	1	0	1	0	0	1	± 550	±275.0
1	1	0/1	1	0	1	0	0	0	±575	±287.5
1	1	0/1	1	0	0	1	1	1	± 600	±300.0
1	1	0/1	1	0	0	1	1	0	±625	±312.5
1	1	0/1	1	0	0	1	0	1	± 650	±325.0
1	1	0/1	1	0	0	1	0	0	±675	±337.5
1	1	0/1	1	0	0	0	1	1	± 700	±350.5
1	1	0/1	1	0	0	0	1	0	±725	±362.5
1	1	0/1	1	0	0	0	0	1	± 750	±375.5
1	1	0/1	1	0	0	0	0	0	±775	±387.5
1	1	0/1	0	1	1	1	1	1	± 800	±400.0
1	1	0/1	0	1	1	1	1	0	±825	±412.5
1	1	0/1	0	1	1	1	0	1	± 850	±425.0

*1 is the "+" or Forward direction

Command T12	T11	Direction* T10	Magnitude T9	T8	T7	T6	T5	T4	Pin Offset Value (microinches) RK06	RK07
1	1	0/1	0	1	1	1	0	0	±875	±437.5
1	1	0/1	0	1	1	0	1	1	± 900	±450.5
1	1	0/1	0	1	1	0	1	0	±925	±462.5
1	1	0/1	0	1	1	0	0	1	± 950	±475.0
1	1	0/1	0	1	1	0	0	0	±975	±487.5
1	1	0/1	0	1	0	1	1	1	± 1000	±500.0
1	1	0/1	0	1	0	1	1	0	±1025	±512.5
1	1	0/1	0	1	0	1	0	1	± 1050	±525.0
1	1	0/1	0	1	0	1	0	0	±1075	±537.5
1	1	0/1	0	1	0	0	1	1	± 1100	±550.5
1	1	0/1	0	1	0	0	1	0	±1125	±562.5
1	1	0/1	0	1	0	0	0	1	± 1150	±575.0
1	1	0/1	0	1	0	0	0	0	±1175	±587.5
1	1	0/1	0	0	1	1	1	1	± 1200	±600.0

*1 is the "+" or Forward direction

APPENDIX B
DRIVE-TO-FTB STATUS MESSAGES

B.1 INTRODUCTION

When the tester is in the exercise mode, the FTB requests and receives messages A0 and B0 only from the drive. This allows the tester to monitor Drive Ready and Drive Fault for errors. If an error message is detected and/or the user wants to view the contents of the other message lines (1, 2, or 3), the status mode can be selected. Upon actuation of the START pushbutton, the FTB requests and receives the message line selected by the MESSAGE SELECT switch. The selected message line status/error bits are then displayed in the MESSAGE A and MESSAGE B LEDs.

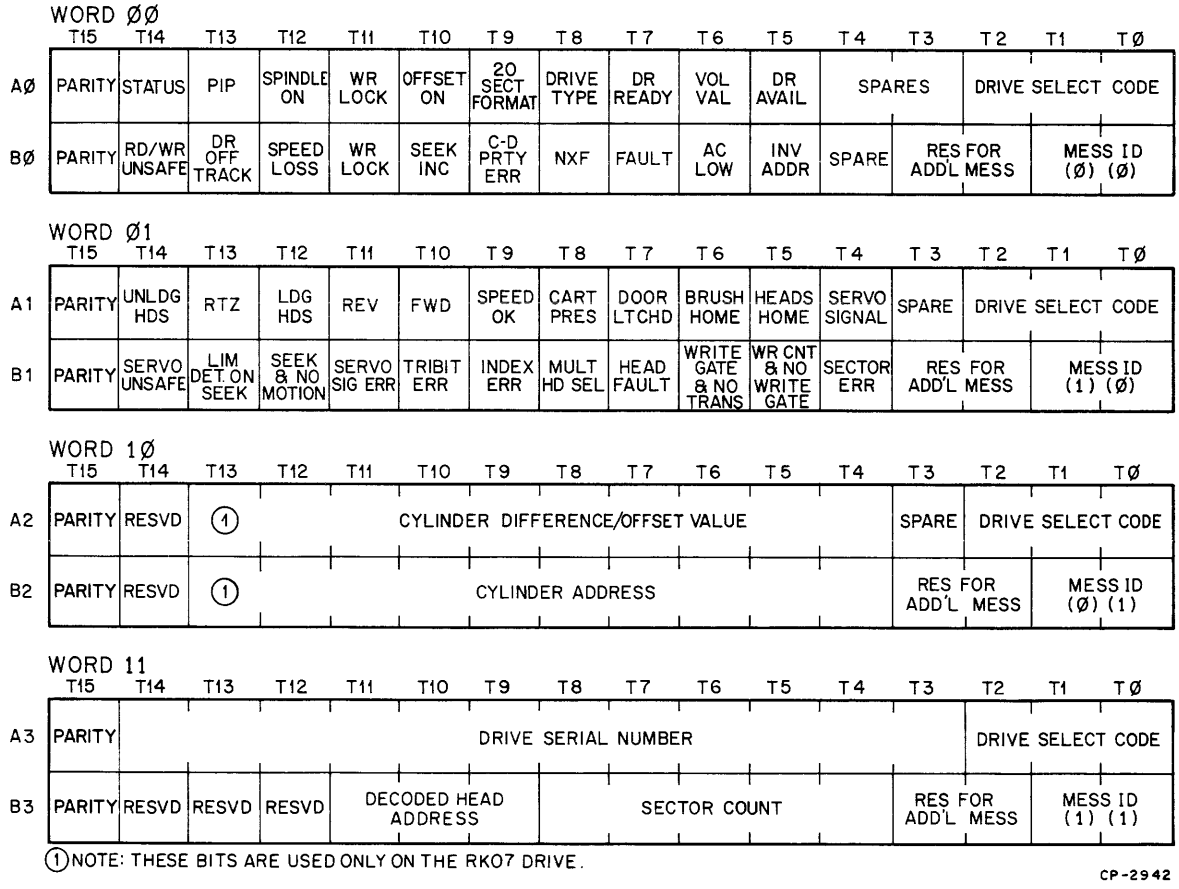


Figure B-1 MESSAGES A and B Drive-to-FTB

B.2 MESSAGE LINE A0

Clock Period	Command	Description
T0 – T2	Selected Drive Address	This binary-encoded address for the selected drive is transmitted as an identification with the least significant bit LSB first. These bits are generated by the contact of the unit select plug.
T3 – T4		No data is transmitted. Consequently, these bits are logical 0.
T5	Drive Available	This bit, when asserted, indicates that the drive is not conducting any operations with another controller. It is for use in dual-access configurations. In single-access configurations, it is always asserted.
T6	Volume Valid (VOL VAL)	This bit is reset by change of cartridge, removal of power, or removal of the unit select plug. It is set by a transmission from the FTB.
T7	Drive Ready	This bit, when asserted, reports that the drive is detented on a cylinder and can receive any command from the FTB.
T8	Drive Type	This bit is designated for transmission of the disk drive type. For the RK06, it is a logical 0 and for the RK07, a logical 1.
T9	Drive Format	This bit is designated for identification of the drive as used for 16- or 18-bit-per-word read/write data and correspondingly 22 or 20 sectors per rotation respectively. When asserted, 18-bit words (20 sectors/rotation) are indicated.
T10	Offset On	This bit indicates that an offset command has been issued to the drive and that the offset has been enabled. The offset flip-flop is set at T14 time of the FTB/DRIVE transmission cycle.
T11	Write Lock	This bit, when asserted, (i.e., set by WRITE PROT switch) reports that the drive is in write lock condition (write protected).
T12	Spindle On	This bit, when asserted, indicates that the selected drive's spindle is energized.
T13	Positioning in Progress	This status bit when asserted is used to indicate that a positioning seek is occurring.

Clock Period	Command	Description
T14	Drive Status Change	This bit is the logical OR of any status change in the selected drive. This status bit is identical to the ATTENTION interface line. The following are the conditions that cause drive status change. 1. The completion of a seek or offset or offset clearing operation 2. The unloading of heads 3. Change of write lock status 4. Any fault condition It is cleared by the drive clear command, initialize, power-up reset, and the run switch reset.
T15	Parity	This bit is the odd parity for the drive to FTB transmission.

B.3 MESSAGE LINE B0

Clock Period	Command	Description
T0 - T1	Message Identifier Bits	These two bits identify this transmission from the drive to FTB and correspond to the message requested on the FTB to drive transmission.
T2 - T3		Reserved for additional message ID bits. Both bits are logical 0.
T4		Reserved, it is a logical 0.
T5	Invalid Address	This bit, when asserted, indicates that the drive has received an invalid head or cylinder address. This bit also asserts fault, drive status change, and attention. When this error occurs, the assertion of fault will prevent any head motion. As a result, the heads are prevented from potentially traveling beyond the limits. This bit is reset by the drive clear, initialize, power-up reset, or the run switch clear.

Clock Period	Command	Description
T6	AC Low Error	This bit, when asserted, reports that a low ac line voltage has been sensed in the drive when the heads are loaded. AC low error is the occurrence of an rms voltage of less than 85 ± 4 V for the low voltage units or 170 ±8 V for the high voltage unit. An ac low condition will cause the heads to unload, beginning with the first sector pulse following ac low detection. This feature allows for the completion of a read or write operation in the current sector. This error is reset by the drive clear, initialize, power-up reset, or the run switch reset provided that ac power has been restored.
T7	Fault	This bit is the logical OR of all of the drive error conditions. The occurrence of fault lights the FAULT indicator on the control panel. The following conditions cause the fault bit to be asserted. 1. More than one drive is selected. 2. Positioner, when detented, has moved too far from its nominal position (e.g., due to the drive being jarred). 3. Parity error is in a control transmission from the FTB to drive. 4. A read/write unsafe condition is in the drive. (Refer to T14 of this message for an explanation the read/write unsafe components.) 5. A write lock error condition exists, (i.e., the receipt of a write gate when the drive is write locked). 6. A low ac voltage is in the drive. 7. A seek incomplete condition exists. 8. A non-executable function exists from the receipt of a write gate or seek command with VOLUME VALID reset. Fault is reset when all of the components are reset.

Clock Period	Command	Description
T8	Non-Executable Function (NXF)	This bit, when asserted, indicates that a seek command or a write gate was received with VOLUME VALID not set. It is reset by the drive clear, initialize, power-up reset, or the run switch reset.
T9	Controller-to-Drive Parity Error	This bit is asserted whenever a parity error occurs in a transmission from the FTB to the drive on either MESSAGE LINE A or B. This error is then reported at this clock time. It is reset by the drive clear, initialize, power-up reset, or the run switch reset.
T10	Seek Incomplete Error	This bit is asserted and transmitted if a seek incomplete occurs. The seek incomplete error occurs whenever the drive fails to successfully complete a seek to a new cylinder. These conditions include the following. 1. A servo unsafe error (see Message B1, T14 for definition). 2. Seek and no motion (see Message B1, T12 for definition). 3. Limit detection seek (see Message B1, T13 for definition). 4. Invalid address (see Message B0, T5 for definition). This error is reset by the drive clear, initialize, power-up reset, or the run switch reset (provided that, if a servo unsafe error occurs, the heads must also be home).
T11	Write Lock Error	This bit, when asserted, reports that the drive has received a WRITE GATE signal when the drive was write protected. It is reset by the drive clear, initialize, power-up reset, or the run switch reset.

Clock Period	Command	Description
T12	Speed Loss Error	This bit, when asserted, indicates that the spindle speed is no longer satisfactory, that the heads are or have unloaded, that no servo unsafe condition exists, and that the spindle motor should be energized. It is cleared by a drive clear, initialize, power-up reset, or the run switch clear (depressing the run switch while heads are home). This bit could be set from such probable causes as the spindle belt falling off or breaking, spindle speed sensor defect, or a problem in spindle motor circuits. Assertion of this bit also asserts fault, drive status change, and attention.
T13	RTZ (Return-to-Zero)	This bit, when asserted, indicates that a recalibrate operation is underway. A recalibration takes place upon command from the contrller or upon dctection of inner limit while loading heads. When (as mentioned above) the inner limit is reached, the heads move in a reverse direction until the outer limit is sensed. At this time, the carriage reverses and moves forward and stops at cylinder 0. When the carriage settles on cylinder 0, this bit is cleared.
T14	Unloading Heads	This bit, when asserted, indicates that the heads are unloadng and are not at the home position.
T15	Parity	This bit is the odd parity bit for this 16-bit byte.

B.4 MESSAGE LINE A1

Clock Period	Command	Description
T0 – T2	Selected Drive Address	The selected drive binary-encoded address is transmitted as an identification with the least significant bit first.
T3		Not used; it is a logical 0.
T4	Servo Signal Present	This bit, when asserted, indicates that the drive heads are loaded and located between the outer and inner limits and that servo signals from the servo surface are being detected.
T5	Heads Home	This bit, when asserted, indicates that the heads are unloaded and at the home position. This bit is generated by the home switch.

Clock Period	Command	Description
T6	Brushes Home	This bit, when asserted, indicates that the disk cleaning brushes are at their home position. This bit is generated by the brushes-home switch.
T7	Door Latched	This bit, when asserted, indicates that the cartridge door is latched. This is generated by the lid locked switch.
T8	Cartridge Present	This bit, when asserted, indicates that a cartridge is present and seated properly in the drive. This bit is generated by the cartridge present switch.
T9	Speed OK	This bit, when asserted, indicates that the disk spindle rotational speed is safe for head loading. This bit is set at a nominal 85 percent of 2400 rev/min
T10	Forward	This bit, when asserted, indicates that the servo has been enabled to move in a forward direction toward the spindle.
T11	Reverse	This bit corresponds to the forward bit, but is for reverse motion.
T12	Heads Loading	This bit, when asserted, indicates that the heads are in the process of loading. In the head loading routine, the heads advance forward until the inner limit is detected. During this time, this bit is asserted. Upon detection of the inner limit, this bit is reset and the RTZ bit, which is reported at T13 time, is asserted.
T13	Drive-Off-Track Error	This bit indicates that a disturbance has caused the head to move an unsafe distance from its nominal detect position while it is in detent mode and wrte gate is asserted or the drive is not ready and receives write gate. For the case where the drive is detented, this error will be sensed if the heads are offset by a nominal 300 μin for a period of at least 0.85 ms. This error is reset by the drive clear, initialize, power-up reset, or the run switch reset.

Clock Period	Command	Description
T14	Read/Write Unsafe	This bit is used for reporting a drive unsafe condition. 1. The drive has been selected along with another in the system. 2. Write current is sensed with no write gate. 3. Write gate is received but there are no write data transitions. 4. A head fault is detected (i.e., a head circuit imbalance is sensed). 5. More than one head has been selected. 6. An index error is detected (i.e., an index has not been sensed or sensed in the wrong location). 7. A tribit error has been sensed (i.e., three successive tribits are missing). 8. Servo signal present error is sensed (i.e., the loss of detection of servo signals from the servo surface). 9. A write gate is coincident with a sector pulse trailing edge. When asserted, the drive unloads the heads but the spindle will not stop. This error is reset by drive clear, initialize, power-up reset, or the run switch reset (provided that the heads are home and the unsafe condition has been cleared).
T15	Parity	This bit is the odd parity bit for this drive-to-FTB transmission.

B.5 MESSAGE LINE B1

Clock Period	Command	Description
T0 - 1	Message Identifier Bits	These two bits identify this transmission from the drive to FTB and correspond to the message requested on the FTB-to-drive transmission with the LSD transmitted first.
T2 - T3		Reserved for additional message ID bits.
T4	Sector Error	This bit, when asserted, indicates that the drive has received write gate coincident with the trailing edge of a sector pulse. This error also causes the read/write unsafe condition and fault. It is cleared by drive clear, initialize, power-up reset, or run switch reset.
T5	Write Current and No Write Gate	This bit, when asserted, indicates that head write current has been detected without a write gate. This error also causes the read/write unsafe condition and fault. It is reset by drive clear, initialize, power-up reset, or run switch reset (provided that the condition has cleared).
T6	Write Gate and No Transitions	This bit reports that the drive has received a write gate signal but has not received any write data. This signal also causes the read/write unsafe condition and fault. It is reset by drive clear, initialize, power-up reset, or run switch reset (provided that the condition has cleared).
T7	Head Fault	This signal, when asserted, indicates that a head fault or head circuit has failed which would cause erroneous data to be recorded on the disk. This error also causes the read/write unsafe condition and fault. It is reset by drive clear, initialize, power-up reset, or run switch reset (provided that the condition has cleared).
T8	Multiple-Head-Select	This bit, when asserted, reports that more than one head is enabled which could cause data to be recorded on more than one surface. This error also causes the read/write unsafe condition and fault. It is reset by drive clear, initialize, power-up reset, or run switch reset (provided the condition has cleared).

Clock Period	Command	Description
T9	Index Error	This bit, when asserted, indicates the absence or misplacement of an index pulse. This condition also causes the read/write unsafe condition and fault. It is reset by drive clear, initialize, power-up reset, or run switch reset.
T10	Tribit Error	This bit, when asserted, indicates the detection of a minimum of three successive tribits are missing. This error also causes the read/write unsafe condition and fault. It is reset by drive clear, initialize, power-up reset, or run switch reset.
T11	Servo Signal Error	This bit, when asserted, indicates the detection of the loss of servo signals from the servo surface. This condition also causes the read/write unsafe condition and fault. It is reset by drive clear, initialize, power-up reset, or run switch reset.
T12	Seek and No Motion Error	This bit, when asserted, indicates that a seek command was issued to the drive, but no track count pulses were detected for 10 ms. This condition represents one of the seek incomplete conditions. It is cleared in the same manner as all errors.
T13	Limit Detection on Seek	This bit, when asserted, indicates that one of the limits was detected during a seek operation. If a limit is detected, the heads will unload, but the spindle will remain on. It is one of the seek incomplete conditions and is cleared in the same manner as all errors.
T14	Servo Unsafe	This bit, when asserted, indicates that the servo amplifier has been saturated for an excessive length of time, thereby indicating a servo runaway condition. This condition causes the heads to do an emergency retract under battery power and stop the spindle. It also causes the seek incomplete condition and is reset in the same manner as all errors once the heads are at home position.
T15	Parity Bit	This bit represents odd parity for this transmission.

B.6 MESSAGE LINE A2

Clock Period	Command	Description
T0 – T2	Selected Drive Address	The binary-encoded address for the selected drive is transmitted as an identification with the least significant bit first. The selected bit reflects the number of the unit select plug.
T3	Reserved	This bit is reserved; it is logical 0.
T4 – T13	Cylinder Difference/Offset Position	These bits represent (all ten on the RK07, but only nine, T4 – T12 on the RK06) represent the binary-encoded cylinder difference that exists during a seek from a seek command and new cylinder address received from the FTB. When the positioner is in detent on a cylinder, these bits represent the offset position if in offset mode. It should be noted that when these bits represent offset status, they are inverted from the input offset bits. This difference is invalid if the drive is seeking and a track-crossing count occurs during the transmission of this count.
T14	Reserved	This bit is reserved. It is a logical 0.
T15	Parity	Parity bit for this 16-bit message.

B.7 MESSAGE LINE B2

Clock Period	Command	Description
T0 – T1	Message Identifier Bits	These two bits identify this transmission from the drive to FTB and correspond to the message requested on the FTB-to-drive transmission with the least significant bit first.
T2 – T3		Reserved for additional message ID bits; both are logical 0.
T4 – T13	Cylinder Address	These bits (all ten on the RK07, but only nine, T4 – T12, on the RK06) report the current cylinder address in binary-encoded form with the least significant bit transmitted first.
T14	Reserved	This bit is reserved. It is a logical 0.
T15	Parity Bit	This bit represents odd parity for this transmission.

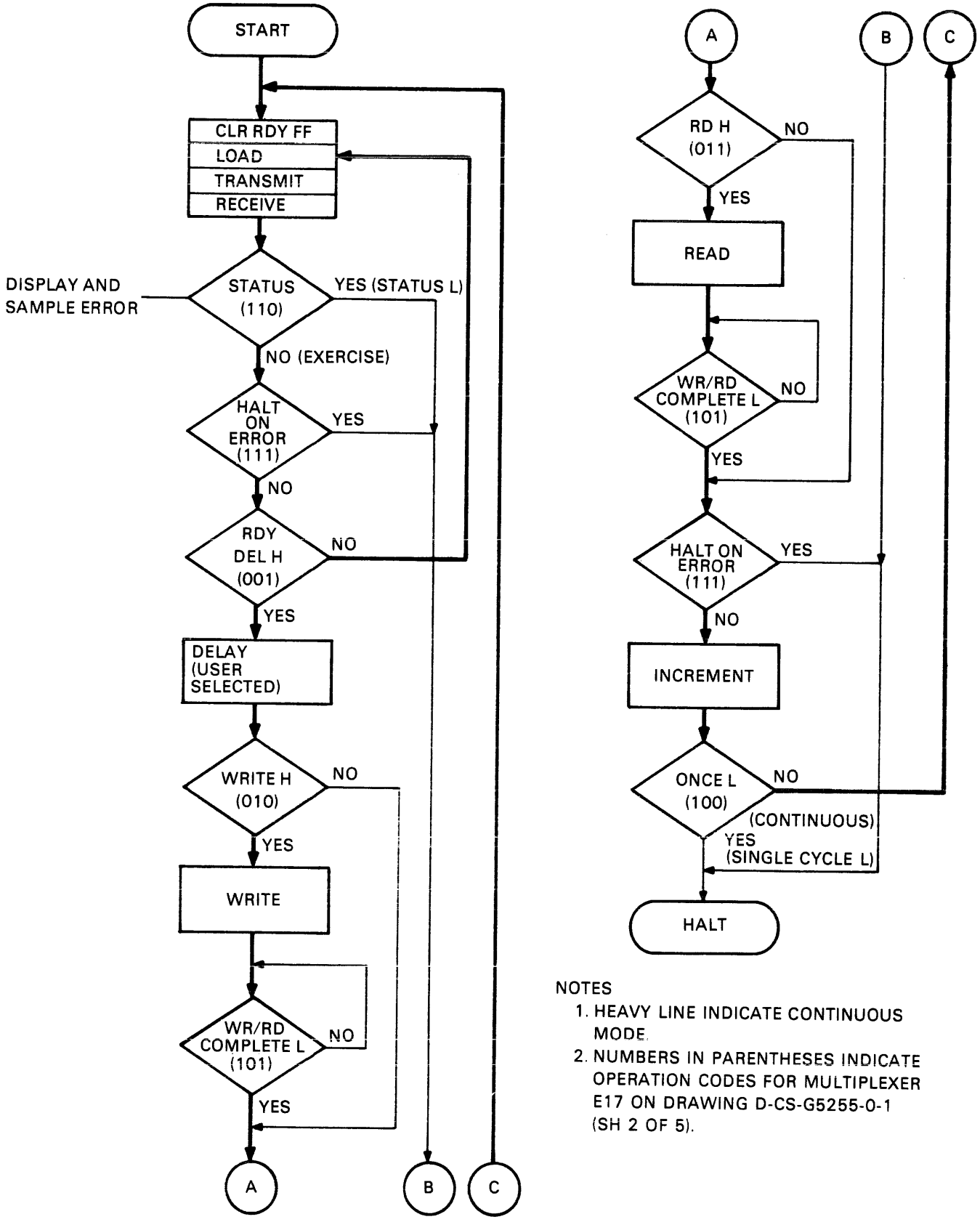
B.8 MESSAGE LINE A3

Clock Period	Command	Description
T0 - T2	Selected Drive Address	The binary-encoded address of the selected drive is transmitted as an identification with the least significant bit first.
T3 - T14	Drive Serial Number	These 12 bits are used to report the three LSD of the drive's serial number. This identification is reported in BCD form with the LSD first and the LSB of each digit first. It is used for error logging purposes.
T15	Parity	This bit represents the parity bit for this 16-bit message.

B.9 MESSAGE LINE B3

Clock Period	Command	Description
T0 - T1	Message Identifier Bits	These two bits identify this transmission from the drive to FTB and correspond to the message requested on the FTB-to-drive transmission.
T2 - T3		These bits are reserved for additional message ID bits. Both are logical 0s.
T14 - T8	Encoded Sector Count	These bits are used for transmitting the present sector address to the FTB. The least significant bit is transmitted first. The sector count is invalid if a sector pulse occurs during these clock times.
T9		Head 0 selected.
T10		Head 1 selected.
T11		Head 2 selected.
T12 - T13	Decoded Head Address	These two bits are reserved; both are logical 0.
T14		Not used.
T15	Parity Bit	This bit is used for transmission of odd parity for this byte.

APPENDIX C
RK6/7 FTB FLOW DIAGRAMS AND BUS MAPS



NOTES

1. HEAVY LINE INDICATE CONTINUOUS MODE.
2. NUMBERS IN PARENTHESES INDICATE OPERATION CODES FOR MULTIPLEXER E17 ON DRAWING D-CS-G5255-0-1 (SH 2 OF 5).

CP-3070

Figure C-1 RK6/7 FTB Flow Diagram

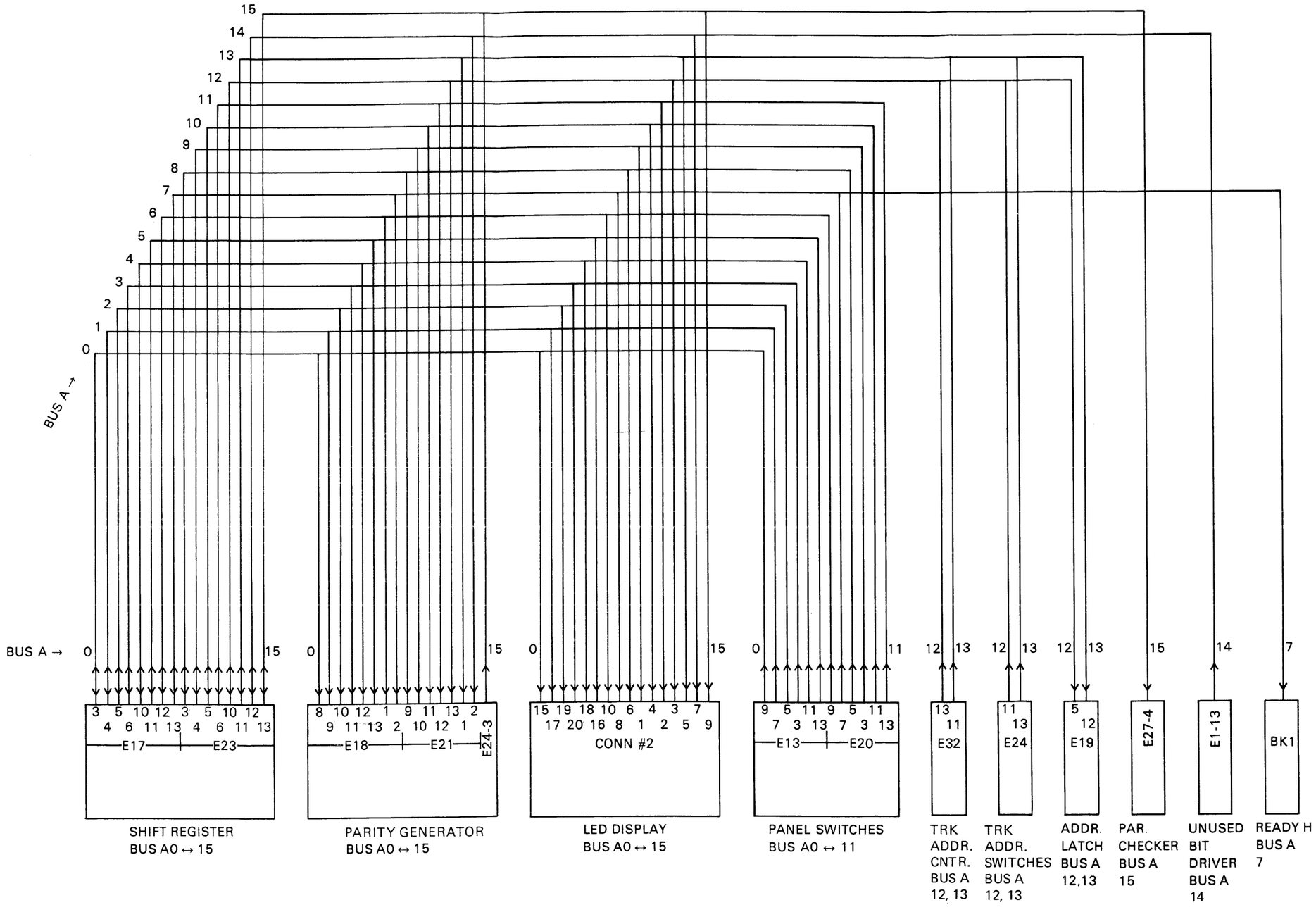


Figure C-2 Field Test Box, Bus A Map

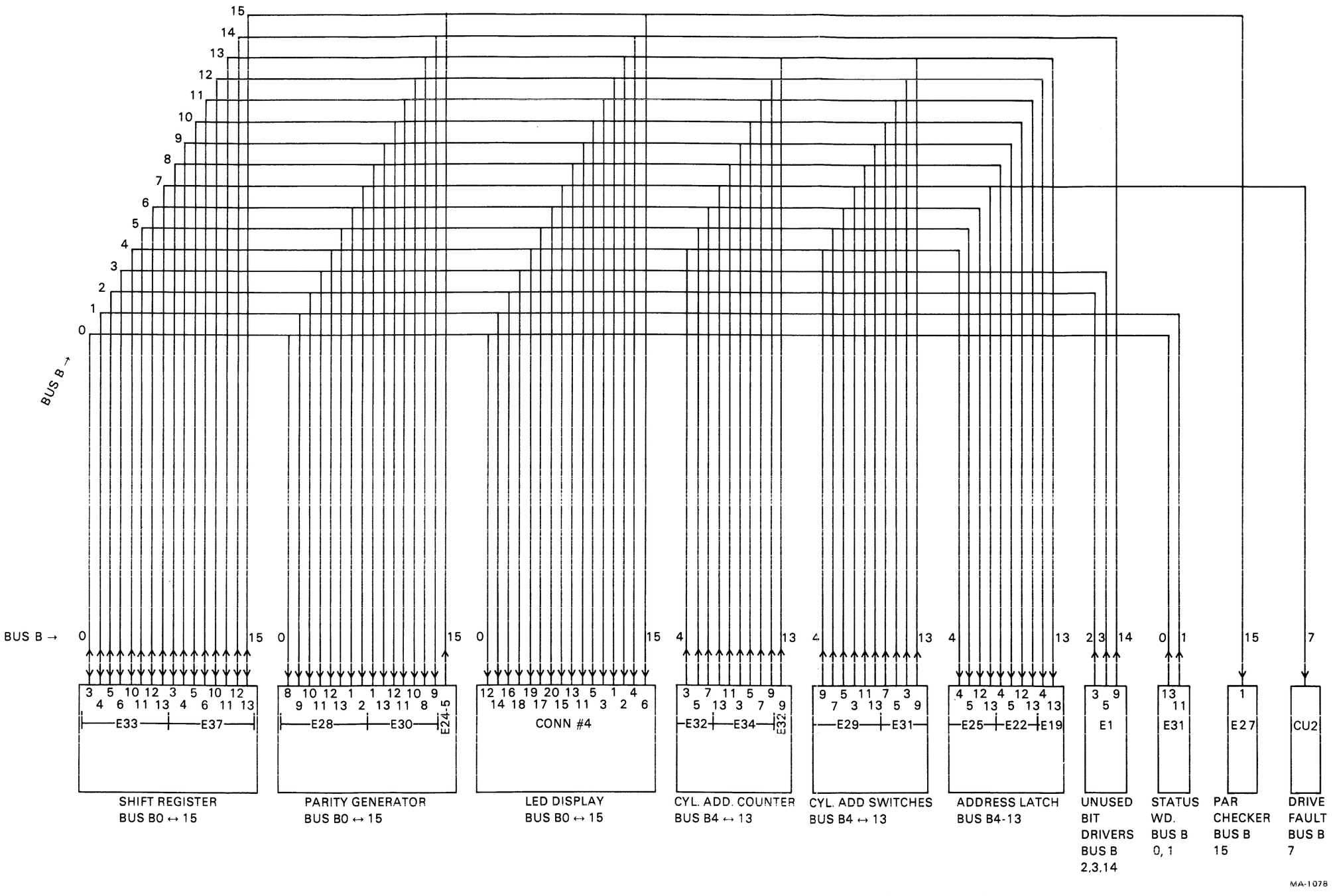


Figure C-3 Field Test Box, Bus B Map

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